MAHATMA GANDHI UNIVERSITY

SCHEME AND SYLLABI

FOR

M. Tech. DEGREE PROGRAMME

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

WITH SPECIALIZATION IN

VLSI & EMBEDDED SYSTEMS

(2011 ADMISSION ONWARDS)
## SCHEME AND SYLLABI FOR M. Tech. DEGREE PROGRAMME
IN ELECTRONICS AND COMMUNICATION ENGINEERING WITH
SPECIALIZATION IN VLSI & EMBEDDED SYSTEMS

### SEMESTER - I

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course No.</th>
<th>Subject</th>
<th>Hrs / Week</th>
<th>Evaluation Scheme (Marks)</th>
<th>Credits (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA</td>
<td>CT</td>
<td>Sub</td>
</tr>
<tr>
<td>1</td>
<td>MEC VE 101</td>
<td>Semiconductor Devices – Physics &amp; Technology</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>MEC VE 102</td>
<td>Advanced Digital System Design</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>MEC VE 103</td>
<td>CMOS VLSI Design</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>MEC VE 104</td>
<td>Embedded System Design</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>MEC VE 105</td>
<td>Elective – I</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>MEC VE 106</td>
<td>Elective – II</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>MEC VE 107</td>
<td>VLSI Design Lab</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>MEC VE 108</td>
<td>Seminar – I</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td>18</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

### Elective – I (MEC VE 105)

- MEC VE 105 - 1: ASIC Design
- MEC VE 105 - 2: High Speed Digital Design
- MEC VE 105 - 3: Low Power VLSI Design
- MEC VE 105 - 4: Semiconductor memories

### Elective – II (MEC VE 106)

- MEC VE 106 - 1: Processor architecture & Parallel processing
- MEC VE 106 - 2: Modeling and Simulation of Electronic System
- MEC VE 106 - 3: System Design Using ARM
- MEC VE 106 - 4: Embedded Networks & Controllers

L – Lecture, T – Tutorial, P – Practical

TA – Teacher’s Assessment (Assignments, attendance, group discussion, Quiz, tutorials, seminars, etc.)

CT – Class Test (Minimum of two tests to be conducted by the Institute)

ESE – End Semester Examination to be conducted by the University

**Electives:** New Electives may be added by the department according to the needs of emerging fields of technology. The name of the elective and its syllabus should be submitted to the University before the course is offered.
## SEMESTER - II

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course No.</th>
<th>Subject</th>
<th>Hrs / Week</th>
<th>Evaluation Scheme (Marks)</th>
<th>Credits (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L  T  P</td>
<td>TA  CT  Sub  Total</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ESE  Total</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>MEC VE 201</td>
<td>Analysis and Design of Analog Integrated Circuits</td>
<td>3 1 0</td>
<td>25 25 50 100 150</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>MEC VE 202</td>
<td>Advanced Embedded System Design</td>
<td>3 1 0</td>
<td>25 25 50 100 150</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>MEC VE 203</td>
<td>VLSI System Design</td>
<td>3 1 0</td>
<td>25 25 50 100 150</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>MEC VE 204</td>
<td>Real Time Operating Systems</td>
<td>3 1 0</td>
<td>25 25 50 100 150</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>MEC VE 205</td>
<td>Elective – III</td>
<td>3 0 0</td>
<td>25 25 50 100 150</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>MEC VE 206</td>
<td>Elective – IV</td>
<td>3 0 0</td>
<td>25 25 50 100 150</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>MEC VE 207</td>
<td>Embedded System Lab</td>
<td>0 0 3</td>
<td>25 25 50 100 150</td>
<td>2</td>
</tr>
<tr>
<td>8</td>
<td>MEC VE 208</td>
<td>Seminar-II</td>
<td>0 0 2</td>
<td>50 0 50 0 50</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Total</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>18 4 5</td>
<td>225 175 400 700 1100 25</td>
<td></td>
</tr>
</tbody>
</table>

**Electives:**
- MEC VE 201-1: DSP System Design
- MEC VE 202-1: MEMS & Micro system technology
- MEC VE 203-1: VLSI Signal Processing
- MEC VE 204-1: Hardware/Software Co Design
- MEC VE 205-2: DSP System Design
- MEC VE 206-2: MEMS & Micro system technology
- MEC VE 207-2: VLSI Signal Processing
- MEC VE 208-2: Hardware/Software Co Design

**Elective – III (MEC VE 205):**
- DSP System Design
- MEMS & Micro system technology
- VLSI Signal Processing
- Hardware/Software Co Design

**Elective – IV (MEC VE 206):**
- Analog & Mixed VLSI circuits
- Testing of VLSI
- CAD for VLSI
- Reconfigurable computing

**L** – Lecture, **T** – Tutorial, **P** – Practical

**TA** – Teacher’s Assessment (Assignments, attendance, group discussion, Quiz, tutorials, seminars, etc.)

**CT** – Class Test (Minimum of two tests to be conducted by the Institute)

**ESE** – End Semester Examination to be conducted by the University

**Electives:** New Electives may be added by the department according to the needs of emerging fields of technology. The name of the elective and its syllabus should be submitted to the University before the course is offered.
### SEMESTER - III

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course No.</th>
<th>Subject</th>
<th>Hrs / Week</th>
<th>Evaluation Scheme (Marks)</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA’</td>
<td>CT</td>
<td>Sub Total</td>
</tr>
<tr>
<td>1</td>
<td>MEC VE 301</td>
<td>Industrial Training or Industrial Training and Mini Project</td>
<td>0</td>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>2</td>
<td>MEC VE 302</td>
<td>Master’s Thesis Phase - I</td>
<td>0</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>30</td>
</tr>
</tbody>
</table>

* TA based on a Technical Report submitted together with presentation at the end of the Industrial Training and Mini Project

** Evaluation of the Industrial Training and Mini Project will be conducted at the end of the third semester by a panel of examiners, with at least one external examiner, constituted by the University.

*** The marks will be awarded by a panel of examiners constituted by the concerned institute

### SEMESTER - IV

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course No.</th>
<th>Subject</th>
<th>Hrs / Week</th>
<th>Evaluation Scheme (Marks)</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA’</td>
<td>CT</td>
<td>Sub Total</td>
</tr>
<tr>
<td>1</td>
<td>MEC VE 401</td>
<td>Master’s Thesis</td>
<td>0</td>
<td>0</td>
<td>30</td>
</tr>
<tr>
<td>2</td>
<td>MEC VE 402</td>
<td>Master’s Comprehensive Viva</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td>30</td>
<td>150</td>
<td>0</td>
</tr>
</tbody>
</table>

Grand Total of all Semesters

<table>
<thead>
<tr>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>2750</td>
</tr>
</tbody>
</table>

* 50% of the marks to be awarded by the Project Guide and the remaining 50% to be awarded by a panel of examiners, including the Project Guide, constituted by the Department

** Thesis evaluation and Viva-voce will be conducted at the end of the fourth semester by a panel of examiners, with at least one external examiner, constituted by the University.
Module 1:
Physics and Properties of Semiconductors - Crystal structure and energy band structure of semiconductors. Carrier concentration and transport, diffusion and drift; Basic semiconductor equations.
P-N Junction Diode – Theory of junction, minority carrier distribution and current components, forward bias, reverse bias, leakage current, breakdown.

Module 2:
Bipolar Transistor. Physics of operation, base transport factor, emitter efficiency, current gain ($\alpha$, $\beta$).
MOSFET - Basic device structures, NMOS, PMOS, operation physics. Parasitic bipolar transistor.

Module 3:
Oxidation technologies in VLSI and ULSI - Kinetics of Silicon dioxide growth both for thick, thin films- High k and low k dielectrics for ULSI- Solid State diffusion modeling and technology; Ion Implantation modeling, damage annealing.

Module 4:
Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI.
CVD techniques for deposition of films; Etching- Evaporation and sputtering techniques- Plasma etching and RIE techniques.

References:
Module -I Synchronous Sequential circuit Design analysis and Optimization

Mealy and Moore model, State machine, Analysis of Synchronous sequential circuit, Design of Sequential Circuit – state equivalence, state reduction, state reduction of incompletely specified state table, State assignment technique. Design of Sequence Generator, Serial Binary Adders.

Module- II Asynchronous Sequential Circuits


Module III Programmable Logic Memory

Memory-ROM, PROM, EPROM, realization of sequential circuit using EPROM. Programmable Logic Devices (PLD)- PLA, PAL, Design using PAL. Gate Array Logic (GAL), design using GAL. EPLD- Altera EP600 EPLD. FPGA- Xilinx FPGA, System development tools for Xilinx FPGA, ACTEL FPGA.

Module IV Digital System Design Using HDL

Introduction to HDL - language elements, expressions, user defined primitives, types of modeling. Design using HDL- Flip flops, Counters, Shift registers, Multiplexers.

References
7. J Bhasker, “A verilog HDL Primer“, PHI
Module 1:
Brief review of NMOS, CMOS, and Bi-CMOS technologies - MOS Transistor theory
CMOS Static logic design - Pseudo-NMOS - Full complementary CMOS - TG gate
CMOS - Pass transistor Logic (PTL) families: DPTL, CPTL - DCVS logic - Realization
using Binary decision diagrams.

Module 2:
CMOS Dynamic logic design - N-P Dynamic logic - Domino logic - NORA logic - TSPC
logic - Multiple output Domino logic - Dynamic NORA dynamic logic circuits - Analysis
of charge charging and noise problems in Dynamic logic circuits - FET scaling in dynamic
logic circuits.

Module 3:
Bi-CMOS static logic design - Standard Bi-CMOS structures - Sub-3V Bi-CMOS
structures - SOI CMOS static logic - Bi-CMOS Dynamic logic design - 1.5V Bi-CMOS
dynamic logic circuit.

Module 4: Timing Issues in Digital Circuits
Technology scaling for sub-micron and deep sub-micron technologies - Design Issues and
Solutions for Deep sub-micron sub-system design.

Characterization and Performance estimation: Design of VLSI Arithmetic Modules
(adders, multipliers) - Area, power and delay estimates - Symbolic layout systems.

References:
2. CMOS VLSI Design Neil H E West, David Harris, Ayan Banerjee, Pearson Edu
3. CMOS Circuit Design, J.P. Uyemura, 1989
4. Sung Mo Kang and Yusuf Lebelci, “CMOS Digital integrated Circuits Analysis and

Module 1:

Module 2: Single-purpose & General purpose processors

Module 3: Peripherals and Interfacing

Module 4: R Introduction to Memory and Embedded System-Case Study

References:
Module 1:

Module 2:
**Programmable ASICS, Programmable ASIC Logic cells** - Anti fuse- static RAM – EPROM and EEPROM technology, PREP benchmarks- Actel ACT-Xilinx LCA- Altera FLEX- Altera MAX – Architecture of FPGAs (Xilinx Spartan-3 – Altera Cyclone-3).

Module 3:

Module 4:

**References:**
5. Cyclone III Device Hand book, Volume 1


Module I
High Speed Digital Design Fundamentals: Frequency and time, Time and distance, Lumped vs distributed, four kinds of reactance- ordinary capacitance and inductance, mutual capacitance and inductance, Relation of mutual capacitance and mutual inductance to cross talk.
High Speed properties of Logic gates: Power, Quicent vs active dissipation, Active power driving a capacitive load, Input power, Internal dissipation, drive circuit dissipation, Totem pole and open circuit speed, Sudden change in voltage and current.

Module II
Measurement Techniques; Rise time and bandwidth of oscilloscope probes, self inductance of probe ground loop, Effects of probe load on a circuit, slow down of a system clock, observing cross talk, measuring operating margin.
Transmission Lines: Problems of point to point wiring, signal distortion, EMI, cross talk, ideal distortion less lossless transmission line, Electrical models of wires.

Module III
Transmission Lines at High frequency: Infinite uniform transmission line, Lossy transmission line, Low loss transmission line, RC transmission line, Skin effect, Mechanics of skin effect, Proximity effect, Dielectric loss, Effects of source and load impedance, Reflections of a transmission line, End termination, Source termination, Very short line

Module IV
Termination: end termination, Rise time, dc biasing, power dissipation, Source termination, Resistance value, Rise time, Power dissipation, Drive current, Middle terminators, Connectors – mutual, series and parasitic capacitance.
Power system: Stable voltage reference, Uniform voltage distribution, resistance and inductance distribution wiring, series resistance and lead inductance of a capacitance
Clock Distribution: schemes, Timing margin, Clock skew, delay adjustments, Clock jitter.
Reference

Module 1: Introduction, Physics of Power Dissipation in CMOS FET Devices

Introduction – Need for VLSI, charging and discharging capacitance, short term current in CMOS circuit, CMOS leakage current, static current, basis principles of low power design, low power figure of merit. Physics of Power Dissipation in MOSFET Devices – power dissipation in CMOS, low power VLSI design limits.

Dynamic Power reduction technique - transition probability minimization, glitch reduction, supply voltage reduction, clock gating, multi-supply design, dynamic voltage and frequency scaling. Transition probability minimization: transition probabilities for some basic gates, inter-signal correlations, logic restructuring, input ordering. Glitching in static CMOS networks.

Module 2: Dynamic & Leakage power reduction technique

Dynamic Power reduction technique - Balanced delay paths to reduce glitching. Supply voltage reduction, power versus voltage, delay versus voltage. Clock gating. Multi-supply design: multiple VDD considerations, optimum numbers of supplies, dual-supply inside a logic block, level shifters, distributing multiple supply voltage: conventional and shared-well.

Dynamic power management vs. Dynamic voltage and frequency scaling. Choosing a frequency in DVFS. Total system energy variation in DVFS.


Module 3: Power Estimation, Synthesis for Low Power, Leakage reduction techniques

Power Estimation – modeling of signals, probabilistic technique for signal activity estimation, statistical techniques, estimation of glitching power, power dissipation in Domino CMOS, power estimation in circuit level, high level power estimation, and estimation of maximum power.
Synthesis for low power - behavioral level transform, logic level optimization for low power, circuit level.

Leakage Reduction techniques - Sleep transistor technique: multi-threshold CMOS (MTCMOS), boosted-gate MOS (BGMOS), sizing of the sleep transistor, super cut-off CMOS (SCCMOS), zigzag super cut-off CMOS (ZSCCMOS). Variable threshold technique: variable threshold CMOS (VTCMOS), VTCMOS versus MTCMOS, dynamic Vth scaling (DVTS), dynamic threshold CMOS (DTMOS), double gate dynamic threshold (DGDT) SOI CMOS.

Module 4: Low Power Logic Styles


References:

Module I RANDOM ACCESS MEMORY TECHNOLOGIES

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs - DRAMs Cell Theory and Advanced Cell Structures- BiCMOS DRAMs-Soft Error Failures in DRAMs- Application Specific DRAMs.

Module II NONVOLATILE MEMORIES
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-EPROMs -Floating-Gate EPROM Cell

Module III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

Module IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

References:


Module 1:

Basic pipelining and Simple RISC Processors: RISC Processors, ISA, examples, basic processor structure, basic pipelining, hazards and solutions, RISC processors-Early Scalar, Sun microSPARC-II, MIPS.

Module 2:

Dataflow Processors: Dataflow verses Control flow, Pure Dataflow, Augmenting Dataflow with Control flow. CISC Processors: Overview, Out-of-order execution, Dynamic scheduling, examples.

Module 3:

Multiple-Issue processors: Overview, I-cache access and Instruction Fetch, Dynamic branch prediction and control speculation, Decode, Rename, issue and dispatch, Execution stages, Finalizing pipelined execution, Principles of VLIW processors – TI TMS320C6x VLIW processors architecture.

Module 4:

Future processors to use Fine-Grain Parallelism, Future processors to use Coarse-Grain Parallelism, Processor in memory, Reconfigurable computing.

References:

1. Processor Architecture From Dataflow to Superscalar and Beyond By Jurij Silc, Borut Robic, Theo Ungerer, Springer.
2. Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, Naim Dahnoun, Prentice Hall
MEC VE 106 - 2  MODELING AND SIMULATION OF ELECTRONIC SYSTEM

Module 1
Foundations : Axioms of arithmetic, proof by contradiction, mathematical induction, figurate numbers, binomial coefficients, Fibonacci numbers, division algorithm, radix representation of a number.
Divisibility : Divisors, greatest common divisor, least common multiple, Euclid’s algorithm, prime factorization, relatively prime numbers, linear Diophantine equations, number and sum of divisors functions, perfect numbers, Mersenne primes,Fermat primes.

Module 2
Linear congruences: congruence relations, congruence arithmetic,complete residue systems, reduced residue systems, Euler’s phi function, linear congruences, Chinese remainder theorem. Polynomial congruences : Polynomial factor theorem, Lagrange’s theorem, quadratic residues, quadratic congruences, Wilson’s theorem, Euler’s criterion.

Module 3
Exponential congruences : Order of an integer modulo n, Fermat’s and Euler’s theorems, roots of unity, primitive roots, indices. Continued fraction algorithm, Pythagorean triples, four-squares theorem, Fermat’s last theorem

Module 4
Introduction-directed and undirected graphs-varieties of graphs-the Königsberg bridge problem-traveling salesman problem-walks, paths and circuits-Euler graphs-Hamiltonian paths and circuits-Trees- panning tree-rooted tree-binary tree -representation of algebraic Structure of binary trees-counting trees-
References:
5. West.DB, “Introduction to Graph Theory” Prentice Hall 1996
Module 1:

**ARM Introduction:** Introduction to processor design-architecture and organization, Abstraction in hardware design, Instruction set design, Processor design trade offs, RISC. Overview of ARM architecture – Architecture inheritance, Programmer’s model, Development tools.

Module 2: ARM Instruction Set:
ARM assembly language programming, ARM organization and implementation, ARM instruction set (exceptions, conditional execution, branching instructions, multiply instructions, coprocessor instructions).

Module 3:
**Architectural support for high level languages**- Data types, Floating point data types, Conditional statements, Loops, Use of memory, Run-time environment

**Thumb instruction set**- Thumb bit, Thumb programmer’s model, Thumb branch instructions, Thumb software interrupt instructions

**Architectural support for system development**- ARM memory interface, AMBA, ARM reference peripheral specifications, h/w system prototyping tools, ARMulator, JTAG, ARM debug architecture, Embedded trace, signal processing support, ARM processor cores.

Module 4:
**Memory heirarachy**- Memory size and speed, On-chip memory, Caches, Memory management.

**Architectural support for OS**- Introduction, ARM system control coprocessor, ARM MMU architecture, Context switching
**Embedded ARM applications**-ARM7500 and ARM 7500FE & The SA-1100 **AMULET**

**asynchronous ARM processors**-Self-timed design & AMULET1.

**References:**

1. ARM System-on-chip architecture, Steve Furber, Pearson Education
2. Computers as Components-principles of Embedded computer system design, Wayne Wolf, Elsevier
3. ARM System Developer’s Guide, Andrew N Sloss, Dominic Symes, Chris Wright, Elsevier
4. An Embedded Software Primer, David E. Simon, Pearson Education.
Module 1: Embedded Networking Requirements

Module 2: Introduction to CAN + CAN Configuration

Module 3: CAN + MICRO CAN + Implementation
CAN-Controller Area Network - Underlying Technology CAN Overview - Selecting a CAN Controller - CAN development tools
MICRO CAN- Implementing CAN open Communication layout and requirements - Comparison of implementation methods - Micro CAN open - CAN open source code - Conformance test - Entire design life cycle.
Implementation- Implementation issues - Physical layer - Data types - Object dictionary - Communication object identifiers - Emerging objects - Node states.

Module 4: Microcontrollers in embedded networks
PIC18FXX8 family, ARM® Cortex™-M3 microcontrollers

References:
3. PIC18FXX8 data sheets
4. ARM® Cortex™-M3 microcontrollers datasheets.
MEC VE 107  
SEMINAR – I

Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the first semester of the M. Tech. programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

MEC VE 108  
VLSI DESIGN LAB

System simulation experiments based on the courses MEC VE 102, MEC VE 103 and the elective courses opted by the student in the first semester.

- HDL based digital design/simulation
- CMOS circuit design/simulation & layout design/simulation
Module 1: MOS transistors

MOS I/V characteristics – Second order effects - MOS modeling in linear, saturation and cutoff - high frequency equivalent circuit – Single stage amplifiers – common source stage – source follower – common gate stage – cascode and folded cascode stage

Module 2:

Differential amplifiers – basic differential pair – common mode response - Basic current mirrors – Cascode current mirrors – Active current mirrors

Module 3:

Frequency response – High frequency modeling - common source stage - source followers - common gate stage - cascode stage - differential pair – CMOS operational amplifiers – one-stage OPAMP – two-stage OPAMP – Need for compensation in OPAMPs – Dominant pole compensation – Pole-zero compensation

Module 4:


References:
Module 1: State machine and concurrent process models
Introduction Models vs. languages, A basic state machine model: finite-state machines (FSM), Finite-state machines with datapath model: FSMD. Using state machines, Hierarchical/Concurrent state machine model (HCFSM) and the Statecharts language, Program-state machine model (PSM), the role of an appropriate model and language, Concurrent process mode: Concurrent processes, Communication among processes, Synchronization among processes, Implementation Dataflow model, Real-time systems.

Module 2: Advanced processors/Controllers (ARM & DSPIC)
Overview of ARM architecture, ARM organization and implementation
DSPIC architecture

Module 3: Device Drivers & Interrupt servicing mechanisms
Device drivers, Parallel port device drivers in a system, Serial port device drivers in a system, device drivers for internals, Interrupt servicing mechanism, context and the periods for context-switching, deadline and interrupt latency

Module 4: Embedded Software development tools
Host and target machines, Linker/locator for embedded software, Getting embedded software into the target systems, debugging techniques, testing on your host machine, instruction set simulators, The assert macro.

References:
4. DSPIC data sheets.
Module 1
Introduction to CAD Tools - Full custom design flow - specification to GDS-II - Types of standard cell elements, design of standard cell library, Study and implementation of standard cell library element.

Module 2

Module 3
VLSI system components circuits-Multiplexers, decoders, Priority encoders, shift registers. Arithmetic circuits- ripple carry adders, carry look ahead adders, high-speed adders, Multipliers.

Module 4
System-on-Chip – Moving to SoC, Overview of SoC design process, Integrating platforms and SoC design, Introduction to Network-on-Chip.

References:


Module 1: Introduction to Embedded System and Real Time Operating system

Basics of developing for embedded systems, Embedded System Initialization, Features of Operating Systems, Introduction to real time operating systems.

Module 2: Kernel Scheduling and Data structures

Tasks, Commonly Used Approaches to Real-Time Scheduling, Semaphores, Message queues, Pipes, Event registers, Signals, Condition Variables.

Module 3: Dealing RTOS design issues

Exceptions and Interrupts, Timer and Timer Services, I/O Subsystem, Memory Management.

Module 4: RTOS porting on Embedded System

Features of Vx Works.

Porting an Operating System like Micro OS or RT Linux on An Embedded Platform.

References:

Module 1
Introduction to a popular DSP from Texas Instruments TMS320C6XXX– CPU Architecture (VLIW) - CPU Data Paths and Control - Timers - Internal Data/ Program Memory - External Memory Interface, Difference between fixed and floating point processors.

Module 2
DSP devices beyond the core, TI C6xxx EVM memory configuration, wait state generator, DMA, Hardware interfacing and I/O control, System management and control.

Module 3

Module 4

References:

Module 1:

Module 2:
MEMS fabrication processes: Review of IC fabrication process, Micromachining: Bulk micromachining (dry and wet etching), Surface micromachining (deposition, evaporation, sputtering, epitaxial growth), Deep RIE, Advanced Lithography, LIGA process; Multi User MEMS Process.

Module 3:

Module 4:
Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD), Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT), Air bag system, Micromotors, Scanning Probe Microscopy.

References:

Module 1:
Representation of DSP algorithms.
Pipelining and Parallel Processing: Introduction, pipelining of FIR filters, parallel processing.

Module 2: Timing Techniques
Retiming: introduction, properties, system inequalities, retiming techniques
Unfolding: Introduction, algorithm, properties, critical path, sample period reduction
Folding: Introduction, Transformation, register minimization

Module 3: DSP Architectures
Systolic architecture design: Introduction, Design Methodologies, FIR systolic array, matrix matrix multiplication.
Parallel FIR filters: Fast FIR, parallel architecture for rank order filters.

Module 4: Pipelining of recursive filters
Introduction, pipeline interleaving, parallel processing in IIR filters, Scaling and round off noise computation, Bit level arithmetic architecture, parallel multipliers, bit serial multipliers, Canonic Singed digit arithmetic, distributed arithmetic.

References:
3. Magdy A Bayoumi, VLSI design methodologies for DSP architecture.
Module 1


Module 2


Module 3


Module 4


References:

Module 1:

Module 2:
Analysis of difference amplifiers with active load using BJT and FET- Supply and Temperature independent biasing techniques-voltage references. Output Stages-Emitter follower-source follower and push pull output stages.

Module 3:
Configuration for Linear IC Current sources-current mirrors- designs-difference amplifiers with active load- biasing techniques-voltage reference-CMOS voltage reference-MOS power amplifier and analog switches-Analog multiplier and PLL-VCO-Closed loop analysis of PLL

Module 4:
MOS switched Capacitor filters-Design-switched capacitor filter-CMOS switched capacitor filters-MOS active RC filters. Mixed signal Design: Delta sigma modulators

References:

Module 1:

Module 2:

Module 3:
Design for testability – Digital DFT and Scan design, Built-in Self test- random logic BIST and memory logic BIST, Boundary Scan standard.

Module 4:

References:


Module 1:
Introduction to VLSI Design methodologies and abstraction levels – Introduction to VLSI design automation tools – Introduction to algorithmic graph theory – Computational complexity – Tractable and Intractable problems - Combinational optimization.

Module 2:

Module 3:

Module 4:
Floor planning concepts – shape functions and floorplan sizing – types of routing problems.

Simulation – gate level modeling and simulation – switch level modeling and simulation.

References:
Module I

Module II
FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms - Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures – Bit Serial.

Module III

Module IV

References:
Each student shall present a seminar on any topic of interest related to the core / elective courses offered in the second semester of the M. Tech. programme. He / she shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.

System simulation experiments based on the courses MEC VE 104, MEC VE 202, MEC VE 204 and the elective courses opted by the student in the second semester.

- Embedded System IDE based simulations
- Real Time applications development
The student shall undergo

i) An Industrial Training of 12 weeks duration in an industry / company / institution approved by the institute under the guidance of a staff member in the concerned field.

OR

ii) Industrial Training of 1 month duration and Mini Project of 2 months duration in an industry / company / institution approved by the institute under the guidance of a staff member in the concerned field. At the end of the training he / she have to submit a report on the work being carried out.

The thesis (Phase - I) shall consist of research work done by the candidate or a comprehensive and critical review of any recent development in the subject or a detailed report of project work consisting of experimentation / numerical work, design and or development work that the candidate has executed.

In Phase - I of the thesis, it is expected that the student should decide a topic of thesis, which is useful in the field or practical life. It is expected that students should refer national & international journals and proceedings of national & international seminars. Emphasis should be given to the introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work / experimentation carried out on the thesis topic. Student should submit two copies of the Phase - I thesis report covering the content discussed above and highlighting the features of work to be carried out in Phase – II of the thesis. Student should follow standard practice of thesis writing. The candidate will deliver a talk on the topic and the assessment will be made on the basis of the work and talks there on by a panel of internal examiners one of which will be the internal guide. These examiners should give suggestions in writing to the student to be incorporated in the Phase – II of the thesis.
In the fourth semester, the student has to continue the thesis work and after successfully finishing the work, he/she have to submit a detailed thesis report. The work carried out should lead to a publication in a National / International Conference. They should have submitted the paper before M. Tech. evaluation and specific weightage should be given to accepted papers in reputed conferences.

A comprehensive viva-voce examination will be conducted at the end of the fourth semester by an internal examiner and external examiners appointed by the university to assess the candidate’s overall knowledge in the respective field of specialization.