Switched Mode Power Converters

(EE364)

S6-EEE

by

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Module 1 - Overview II

- Continuous Conduction Mode
- Boundary between CCM and DCM
- Discontinuous Conduction Mode
- Output Voltage Ripple
- Effect of Parasitic Elements

1. Introduction

- **DC-DC Converters** : Unregulated dc input $\rightarrow$ Controlled dc output

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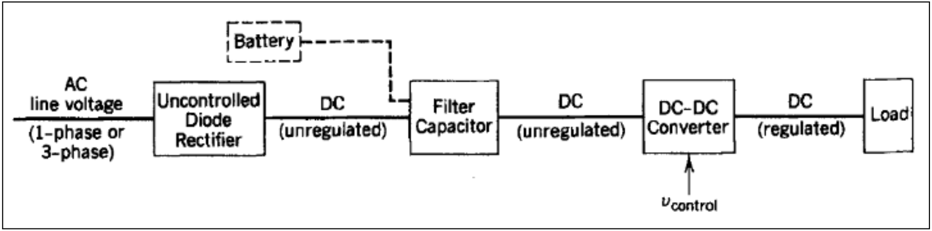

Figure 1 : DC-DC Converter System

- **Assumptions**
  - Steady State Analysis

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  - Ideal Switches

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  - Filter at output side of the converter

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Control Schemes

1. Pulse Width Modulation (PWM) switching
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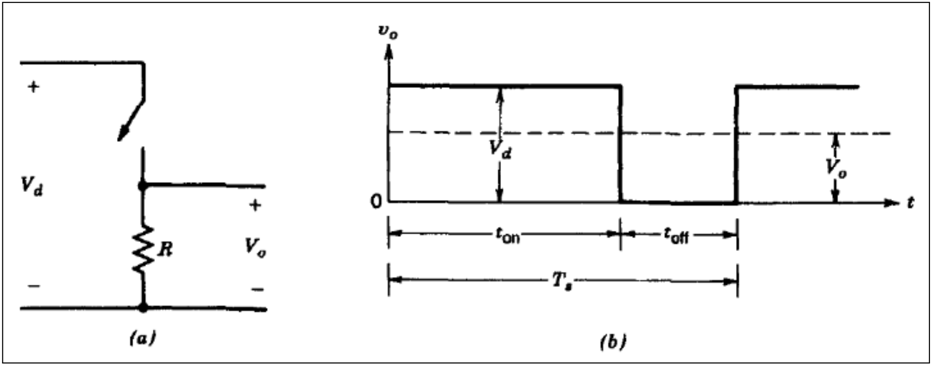
2. By varying both f_{sw} and t_{on}
   - T_s and D are varied
   - Used only in dc-dc converters with force-commutated thyristors
   - Variation in f_{sw} $\rightarrow$ difficult to filter ripple components in the output.



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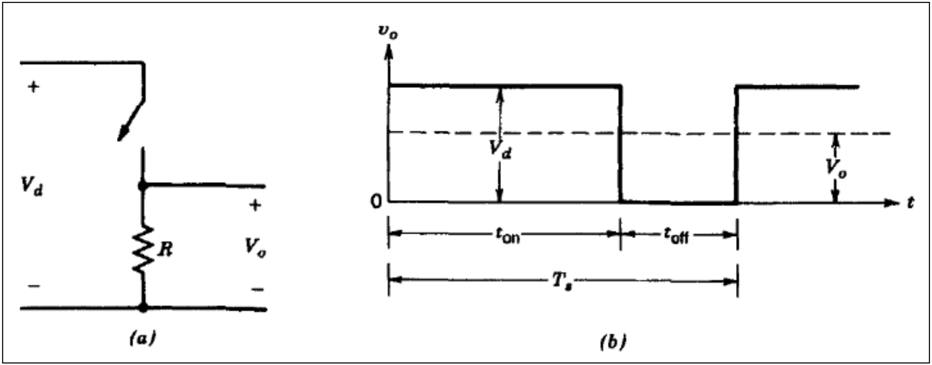
Pulse Width Modulation (PWM) switching



- Gate signals are generated by comparing $v_{control}$ with repetitive waveform
- Repetitive waveform
  - Sawtooth waveform
  - Constant peak
  - f_{sw}

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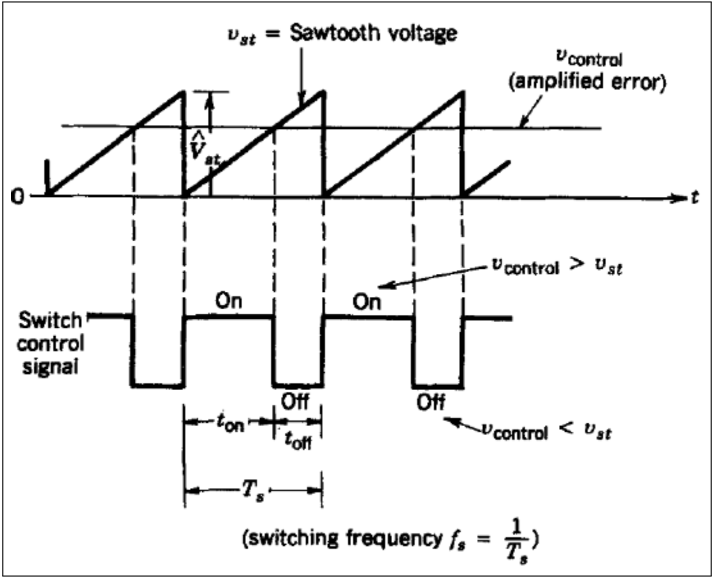

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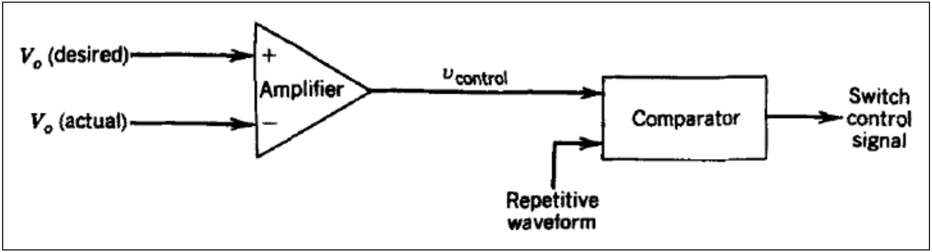
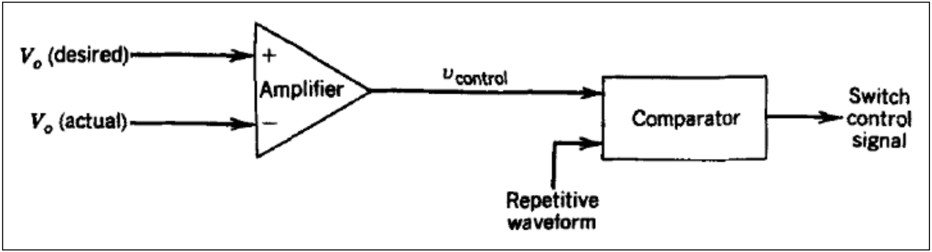


- When $v_{control} > v_{st} \rightarrow$ Switch is ON
- When $v_{control} < v_{st} \rightarrow$ Switch is OFF



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- When $v_{control} < v_{st} \rightarrow$ Switch is OFF
- Duty Ratio

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\hat{V}_{st}}$$

- **Step-down converter**
- $V_o < V_d$

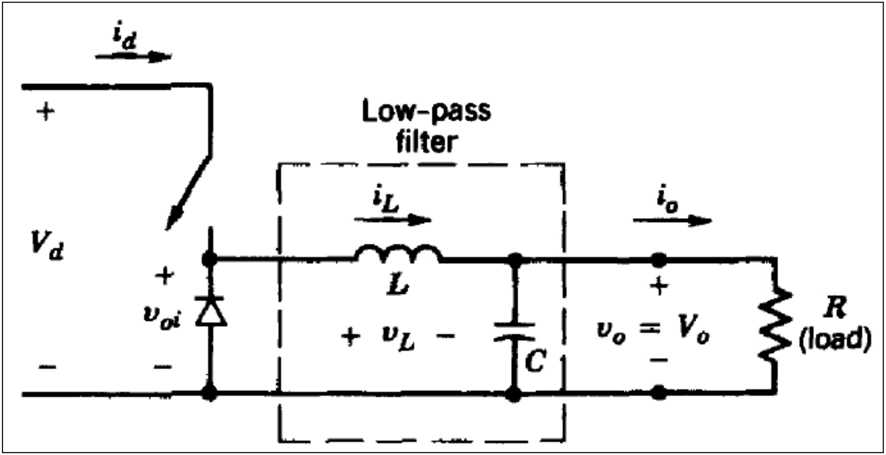

Figure 2 : Buck Converter

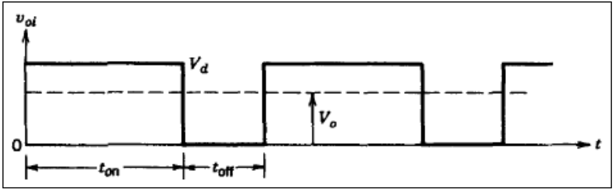

Figure 3 : Output Voltage

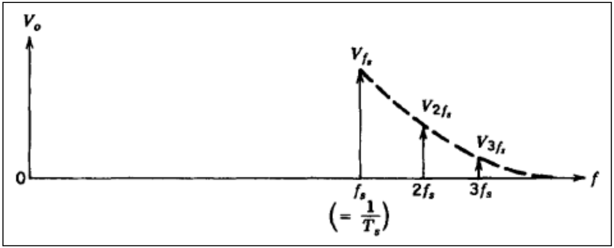

Figure 4 : Frequency spectrum of v_{oi}

- Average output voltage

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)\,dt = \frac{1}{T_s}\left(\int_0^{t_{on}} V_d\,dt + \int_{t_{on}}^{T_s} 0\,dt\right) = \frac{t_{on}}{T_s}V_d = DV_d$$

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- V_o varies **linearly** with the control voltage ($v_{control}$)
- Diode helps to dissipate the stored energy in inductor
- Output voltage fluctuates between 0 and V_d
- Output voltage fluctuations are diminished by using a low-pass filter

Operation

- When switch is **ON**
    - Diode becomes revere biased
    - Input provides energy to load & inductor
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- When switch is **OFF**
  - Inductor current flows through diode and load
- If filter capacitor is very high $\implies v_o \approx V_o$
- Average Inductor current $=$ Average output current (I_o)
  - Since average capacitor current in steady state is zero

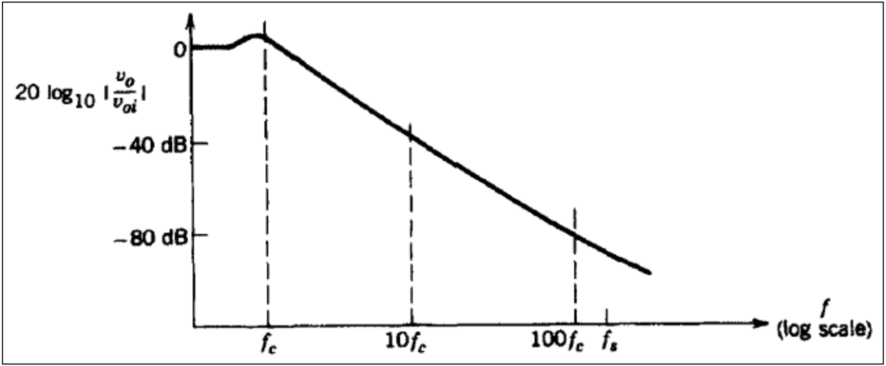

Figure 5 :

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- Inductor current, $i_L(t)$ flows continuously
- $i_L(t) > 0$

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Operation

- When Switch is ON
  - Diode becomes reverse biased
  - $v_L = V_d - Vo$
  - Linear increase in i_L
- When Switch is OFF
  - i_L continues to flow due to inductor stored energy
  - i_L flows through diode
  - $v_L = -V_o$

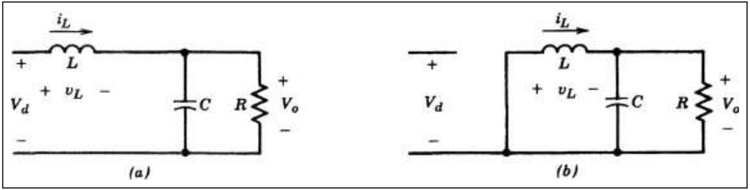
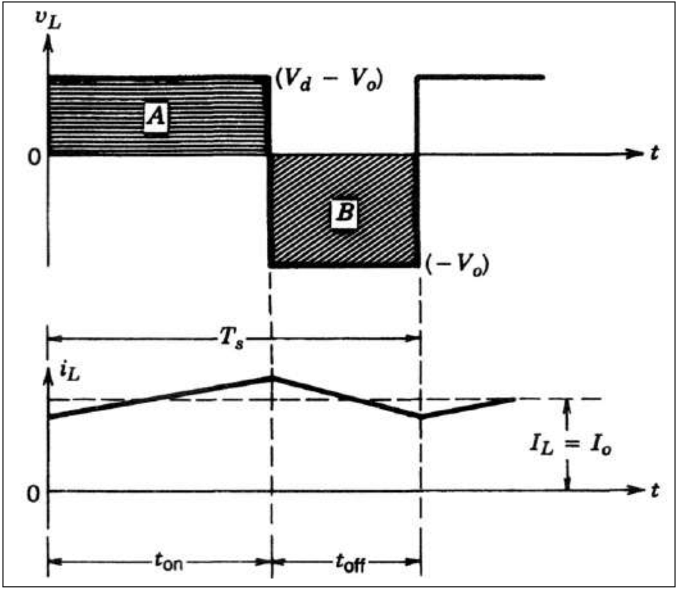


Figure 6: Buck Converter (a) Switch ON (b) Switch OFF

3.1 Continuous Conduction Mode



- Integral of inductor voltage (v_L) over one time period (T_s) must be zero

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$$\frac{V_o}{V_d} = \frac{t_{on}}{T_s} = D \quad \text{(duty ratio)}$$

- Output voltage varies linearly with the duty ratio of the switch for a given input voltage and it **does not depend on any other circuit parameter**

- Neglecting the power losses,

$$P_d = P_o$$

$$V_d I_d = V_o I_o$$

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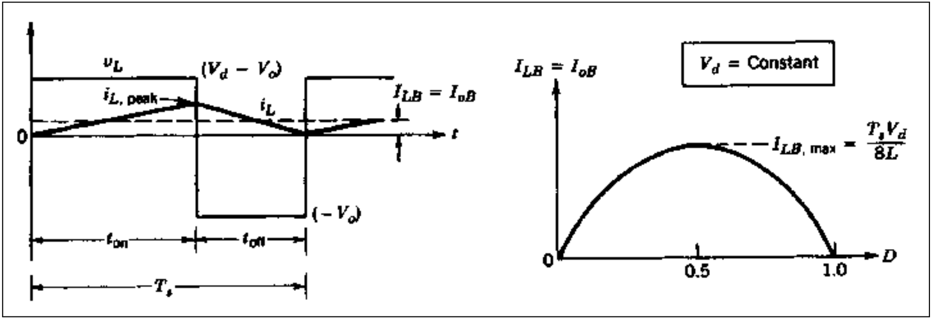
- In continuous-conduction mode, Buck converter is equivalent to a dc voltage regulator where duty ratio can be continuously controlled electronically in a range of 0 to 1.

- i_L goes to zero at the end of OFF period



- Boundary condition

$$I_{LB} = \frac{1}{2} i_{L,\text{peak}} = \frac{t_{\text{on}}}{2L}(V_d - V_o) = \frac{DT_s}{2L}(V_d - V_o) = I_{oB}$$

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- With a given set of values for T_s, V_d, V_o, L and D, if the average inductor current (I_L) becomes less than I_{LB}, then i_L will become **discontinuous**.

Modes

- Constant input voltage (V_d)
- Constant output voltage (V_o)

- **DC motor speed control**
  - V_d remains constant & V_o is controlled by adjusting the converter duty ratio D
- Average inductor current at the edge of continuous-conduction mode

$$I_{LB} = \frac{T_s V_d}{2L} D(1 - D)$$

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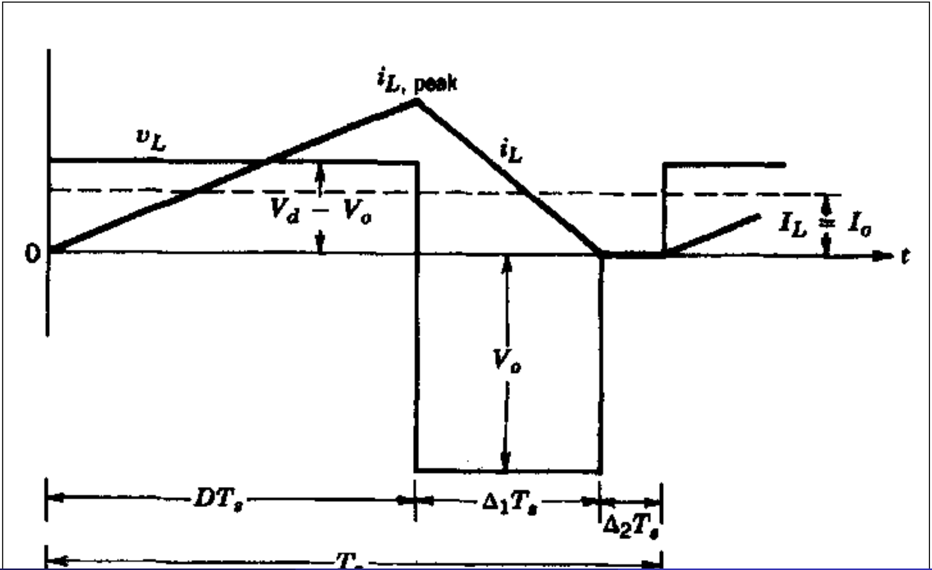
$$I_{LB,\max} = \frac{T_s V_d}{8L}$$

$$I_{LB} = 4 I_{LB,\max} D(1 - D)$$



$i_{L,\text{ peak}}$
v_L
i_L
$V_d - V_o$
0
$I_L = I_o$
t
V_o
DT_s
$\Delta_1 T_s$
$\Delta_2 T_s$
T_s

Operation

- Assume that initially converter is operating at the edge of continuous conduction for given values of T, L, V_d, and D
- Decrease output load power (i.e. increase load resistance)
- Then I_L will decrease
- Higher value of V_o than before and results in a discontinuous inductor current

Discontinuous Conduction Mode with Constant V_d

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During **discontinuous period ($\Delta_2 T_s$)**

- $i_L = 0$, $v_L = 0$
- Power to load is supplied by filter capacitor alone

- Integral of inductor voltage over one time period = 0

Discontinuous Conduction Mode with Constant V_d

- Integral of inductor voltage over one time period = 0

$$(V_d - V_o)\,DT_s + (-V_o)\Delta_1 T_s = 0$$

$$\therefore \frac{V_o}{V_d} = \frac{D}{D + \Delta_1}$$

where $D + \Delta_1 < 1$

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$$i_{L,\text{peak}} = \frac{V_o}{L}\Delta_1 T_s$$

Discontinuous Conduction Mode with Constant V_d

$$I_o = i_{L,\text{peak}} \frac{D + \Delta_1}{2}$$

$$= \frac{V_o T_s}{2L}(D + \Delta_1)\,\Delta_1$$

$$= \frac{V_d T_s}{2L} D\Delta_1$$

$$= 4I_{LB,\max} D\Delta_1$$

$$\therefore\ \Delta_1 = \frac{I_o}{4I_{LB,\max} D}$$

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$$\frac{V_o}{V_d} = \frac{D^2}{D^2 + \frac{1}{4}(I_o / I_{LB,\max})}$$

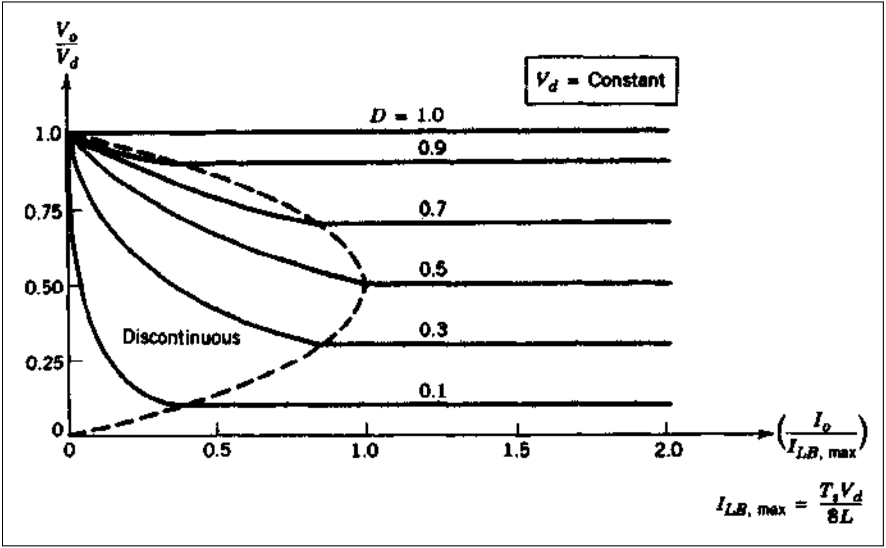

Figure 7 : Step-down converter characteristics keeping $V_d$constant

Discontinuous Conduction Mode with Constant V_d

- In figure 7, voltage ratio (V_o/V_d) is plotted as a function of $(I_o/I_{LB,max})$ for various values of duty ratio (D)
- Dashed curve shows the boundary between continuous and discontinuous modes.

Discontinuous Conduction Mode with Constant V_o

- In **regulated dc power supplies**, V_d may fluctuate but V_o is kept constant by adjusting the duty ratio (D)
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- If V_o is kept constant, the maximum value of I_{LB} occurs at D = 0

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$$I_{LB,\max} = \frac{T_s V_o}{2L}$$

- Converter operation with D = 0 and a finite V_d is **hypothetical**

$$I_{LB} = (1 - D) I_{LB,\max}$$

- For the converter operation where V_o is kept constant, the required duty ratio (D) can be obtained as

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$$D = \frac{V_o}{V_d}\left(\frac{I_o/I_{LB,max}}{1 - V_o/V_d}\right)^{1/2}$$

- The duty ratio (D) as a function of $I_o/I_{LB,max}$ is plotted in figure 8 for various values of (V_d/V_o) keeping V_o constant
- Dashed curve shows the boundary between continuous and discontinuous modes.

Discontinuous Conduction Mode with Constant V_o

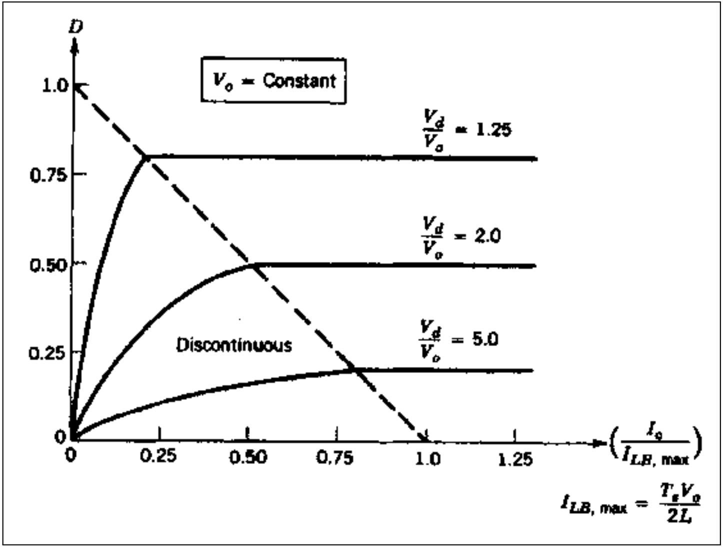

Figure 8 : Step-down converter characteristics keeping V_o constant

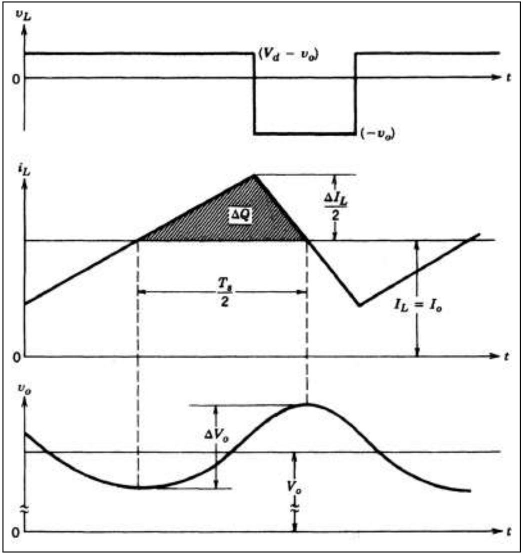

Figure 9 : Output voltage ripple in Buck Converter

3.4 Output Voltage Ripple

- **Assumption** : If output capacitor is so large, $v_o(t) = V_o$
- But in practical circuits, there will be **ripple in the output voltage**
- The shaded area in figure 9 represents an additional charge ΔQ
- For a continuous conduction mode of operation, assuming that all of the ripple component in i_L flows through the capacitor and its average component flows through the load resistor, peak to peak voltage ripple (ΔV_o) can be calculated as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\Delta I_L}{2}\frac{T_s}{2}$$

During t_{off}

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During t_{off}

$$\Delta I_L = \frac{V_o}{L}(1 - D)T_s$$

3.4 Output Voltage Ripple

$$\Delta V_o = \frac{T_s}{8C}\frac{V_o}{L}(1 - D)T_s$$

$$\therefore \frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1 - D)}{LC} = \frac{\pi^2}{2}(1 - D)\left(\frac{f_c}{f_s}\right)^2$$

where f_s = Switching frequency and f_c = Corner frequency of LPF

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- Voltage ripple can be minimized by selecting a corner frequency (f_c) of the low-pass filter at the output such that $f_c << f_s$

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

- Voltage ripple is independent of the output load power, so long as the converter operates in the continuous conduction mode
- In switch-mode dc power supplies, the percentage ripple in the output voltage is usually specified to be less than 1%

4. Boost Converter

- **Regulated DC Power Supplies** and **Regenerative Braking of DC Motors**
- Output voltage is always greater than the input voltage

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Operation

- When switch is **ON**
  - Diode is reversed biased
  - Output stage is isolated
  - Input supplies energy to the inductor
- When switch is **OFF**
  - Output stage receives energy from the inductor as well as from the input
- In steady state analysis, the output filter capacitor is assumed to be very large to ensure a constant output voltage ie, $v_o(t) = V_o$

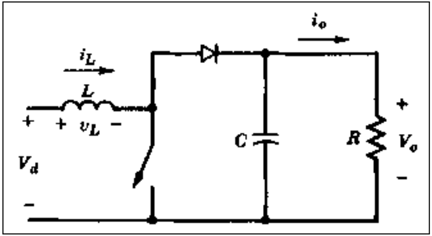

Figure 10 : Boost Converter

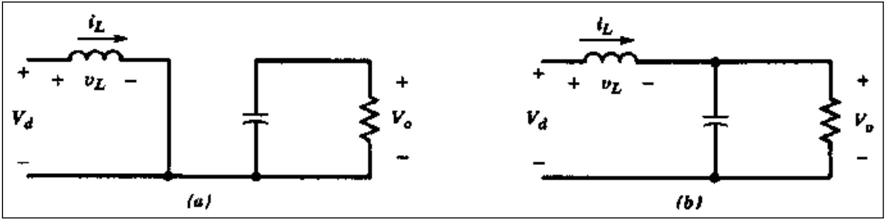

Figure 11 : CCM (a) When Switch is **ON** (b) When Switch is **OFF**

4.1 Continuous Conduction Mode

- **CCM** $\rightarrow$ Inductor current flows continuously ie, $i_L(t) > 0$
- In steady state, the time integral of the inductor voltage over one time period must be zero

$$V_d t_{\text{on}} + (V_d - V_o) t_{\text{off}} = 0$$

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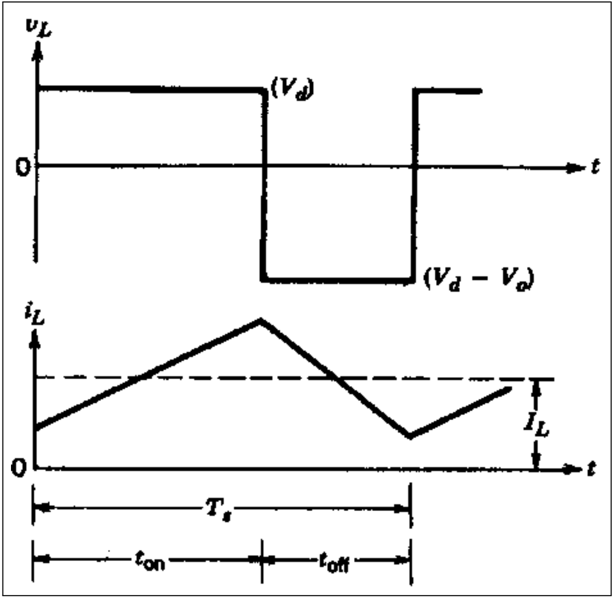
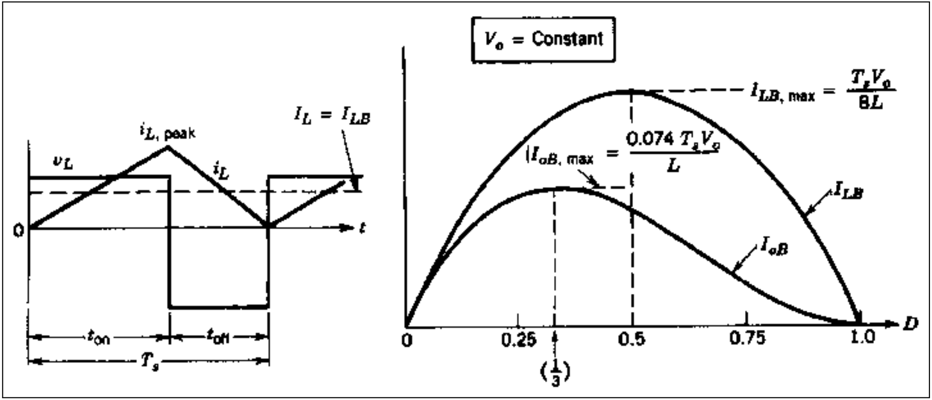
$$P_d = P_o, \qquad \therefore V_d I_d = V_o I_o$$

$$\frac{I_o}{I_d} = (1 - D)$$



v_L
(V_d)
0
t
$(V_d - V_o)$
i_L
I_L
0
t
T_s
t_{on}
t_{off}

- i_L goes to zero at the end of OFF interval



- Average inductor current at boundary (I_{LB})

- Average inductor current at boundary (I_{LB})

$$\begin{aligned} I_{LB} &= \frac{1}{2} i_{L,\text{peak}} \\ &= \frac{1}{2} \frac{V_d}{L} t_{\text{on}} \\ &= \frac{T_s V_o}{2L} D(1 - D) \end{aligned}$$

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- In Boost converter, inductor & input currents are same. ie, $i_L = i_d$
- Average output current at the edge of continuous conduction,

4.2 Boundary between CCM and DCM

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- In Boost converter, inductor & input currents are same. ie, $i_L = i_d$
- Average output current at the edge of continuous conduction,

$$I_{oB} = \frac{T_s V_o}{2L} D(1 - D)^2$$

- Keeping V_o constant and varying the duty ratio (D) imply that the input voltage (V_d) is varying
- I_{LB} reaches maximum value at D = 0.5

$$I_{LB,\max} = \frac{T_s V_o}{8L}$$

- I_{oB} has its maximum at D = 1/3 = 0.333

$$I_{oB,\max} = \frac{2}{27}\frac{T_s V_o}{L} = 0.074\,\frac{T_s V_o}{L}$$

$$I_{LB} = 4D(1-D)I_{LB,\max}$$

$$I_{oB} = \frac{27}{4} D(1 - D)^2 I_{oB,\max}$$

- For a given D, with constant V_o, if the average load current (I_o) drops below (I_{oB}), OR ($i_L < i_{LB}$), the current conduction will become discontinuous

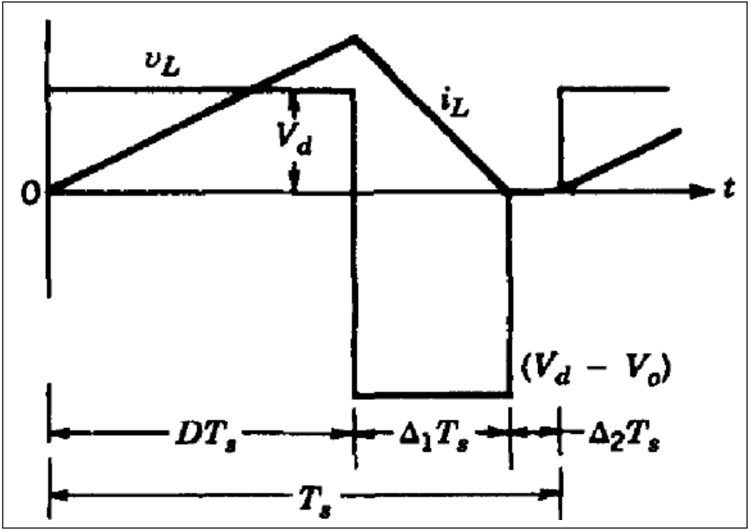

Figure 12 : Boost converter at discontinuous conduction

- Assume that as the output load power decreases, V_d and D remain constant
- Discontinuous current conduction occurs due to decreased P_o $(=P_d)$ and hence a lower I_L $(=I_d)$ since V_d is constant
- i_{Lpeak} is same in both modes. Hence a lower value of I_L (and hence a discontinuous i_L) is possible only if V_o goes up
- Integral of inductor voltage over one time period is zero

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- Integral of inductor voltage over one time period is zero

$$V_d D T_s + (V_d - V_o)\Delta_1 T_s = 0$$

$$\boxed{\frac{V_o}{V_d} = \frac{\Delta_1 + D}{\Delta_1}}$$

4.3 Discontinuous Conduction Mode

- Since $P_d = P_o$

$$\frac{I_o}{I_d} = \frac{\Delta_1}{\Delta_1 + D}$$

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$$I_d = \frac{V_d}{2L} DT_s(D + \Delta_1)$$

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- Average input current (I_d) = Average inductor current (I_L)

$$I_d = \frac{V_d}{2L} DT_s(D + \Delta_1)$$

$$I_o = \left(\frac{T_s V_d}{2L}\right) D\Delta_1$$

- Since V_o is held constant and D varies in response to the variation in V_d,

$$D = \left[\frac{4}{27}\frac{V_o}{V_d}\left(\frac{V_o}{V_d}-1\right)\frac{I_o}{I_{oB,\max}}\right]^{1/2}$$

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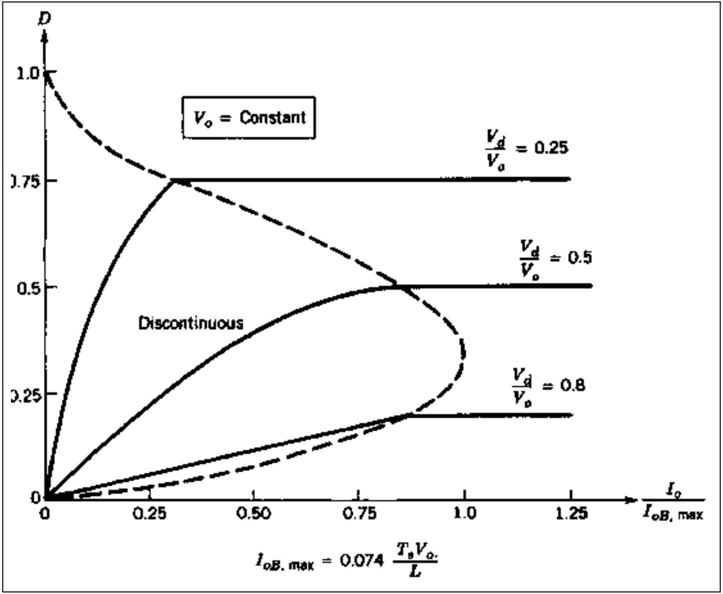
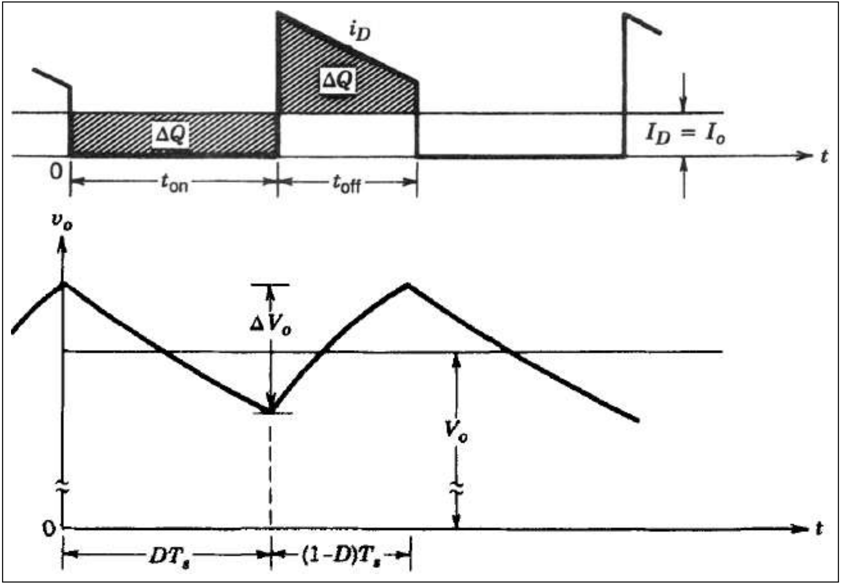
$$D = \left[\frac{4}{27}\frac{V_o}{V_d}\left(\frac{V_o}{V_d} - 1\right)\frac{I_o}{I_{oB,\max}}\right]^{1/2}$$

- In discontinuous mode, if V_o is not controlled during each switching time period, energy will be transferred from the input to the output capacitor and to the load

$$\frac{L}{2} i^2_{L,\text{peak}} = \frac{(V_d D T_s)^2}{2L} \qquad \text{W-s}$$

- If the load is not able to absorb this energy, the capacitor voltage V_c $(= V_o)$ would increase until an energy balance is established. If the load becomes very light, the increase in V_o, may cause a **capacitor breakdown or a dangerously high voltage to occur**.


D
1.0
0.75
0.5
0.25
0
V_o = Constant
$\frac{V_d}{V_o}$ = 0.25
$\frac{V_d}{V_o}$ = 0.5
$\frac{V_d}{V_o}$ = 0.8
Discontinuous
0
0.25
0.50
0.75
1.0
1.25
$\frac{I_o}{I_{oB,\,max}}$
$I_{oB,\,max} = 0.074\,\frac{T_s V_o}{L}$



i_D
ΔQ
ΔQ
$I_D = I_o$
t
0
t_{on}
t_{off}
v_o
ΔV_o
V_o
0
t
DT_s
$(1-D)T_s$

4.4 Output Voltage Ripple

- Assume that all the ripple current component of the diode current (i_D) flows through the capacitor and it's average value flows through the load resistor

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$$\Delta V_o = \frac{\Delta Q}{C} = \frac{I_o D T_s}{C}$$

$$= \frac{V_o}{R} \frac{D T_s}{C}$$

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$$= \frac{V_o}{R} \frac{D T_s}{C}$$

$$\frac{\Delta V_o}{V_o} = \frac{D T_s}{RC}$$

$$= D \frac{T_s}{\tau}$$

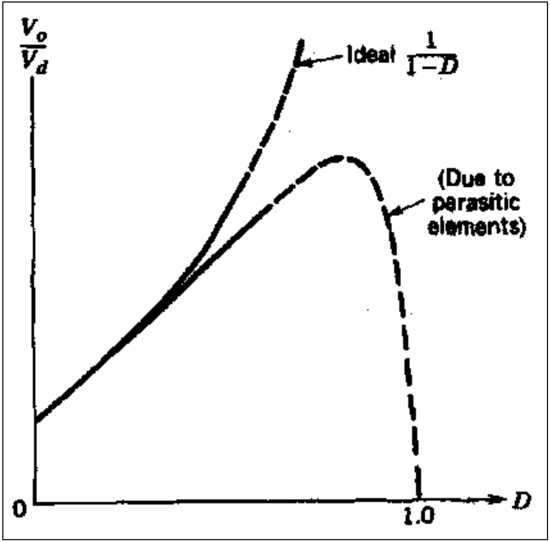

Figure 13 : Effect of parasitic elements on D

4.5 Effect of Parasitic Elements

- Parasitic elements are due to the losses associated with the inductor, capacitor, switch and the diode
- Unlike ideal characteristic, in practice, (V_o/V_d) declines as 'D' approaches unity
- Very poor switch utilization at high values of duty ratio

Q) In a step-up converter, the duty ratio is adjusted to regulate the output voltage at 48 V. The input voltage varies in a wide range from 12 to 36 V. The maximum power output is 120 W. For stability reasons, it is required that the converter always operate in a discontinuous-current-conduction mode. The switching frequency is 50 kHz. Assuming ideal components and C as very large, calculate the maximum value of L that can be used.

Problem

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$$L = \frac{20 \times 10^{-6} \times 48}{2 \times 2.5} 0.75(1 - 0.75)^2$$
$$= 9\ \mu H$$

- **Regulated DC power supplies**
- Negative polarity output with respect to the common terminal of the input voltage
- Output voltage can be either higher or lower than the input voltage
- Cascade connection of Buck and Boost converters → **Buck-Boost Converter**

$$\frac{V_o}{V_d} = D \frac{1}{1 - D}$$

- Output voltage can be higher or lower than the input voltage, based on the duty ratio

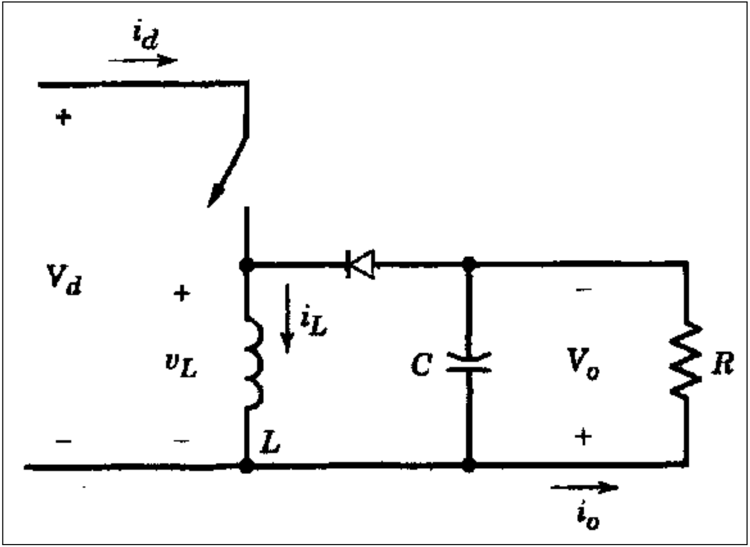


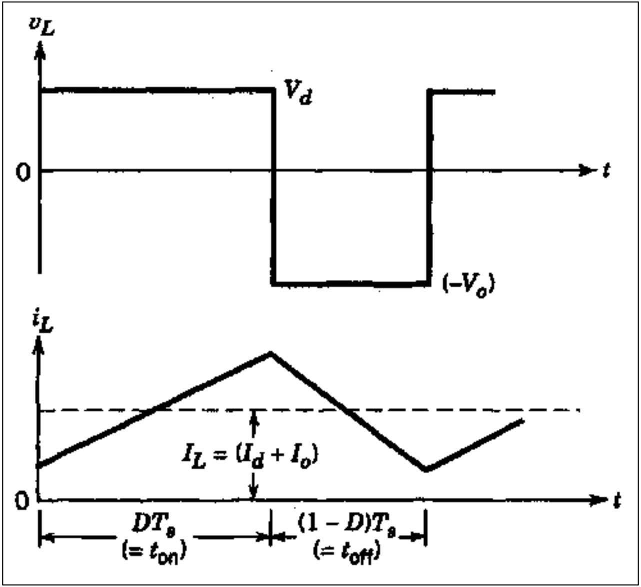
Figure 14 : Buck-Boost Converter

Operation

- When switch is **ON**
  - Input provides energy to the inductor
  - Diode is reverse biased
- When switch is **OFF**
  - Energy stored in the inductor is transferred to the output
  - No energy is supplied by the input

- In steady-state analysis, the output capacitor is assumed to be very large $\implies v_o(t) = V_o$

5.1 Continuous Conduction Mode



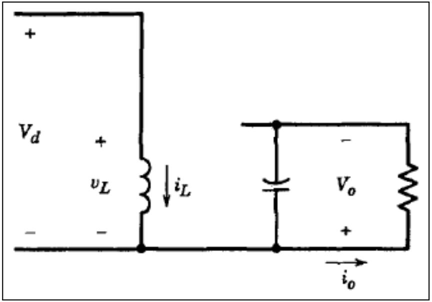


Figure 15 : Buck-Boost Converter : Switch is ON

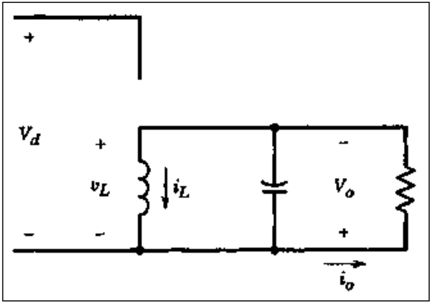


Figure 16 : Buck-Boost Converter : Switch is OFF

- Inductor current flows continuously
- Integral of inductor voltage over one time period is zero $\implies$

- Inductor current flows continuously
- Integral of inductor voltage over one time period is zero $\implies$

$$V_d D T_s + (-V_o)(1 - D)T_s = 0$$

$$\boxed{\frac{V_o}{V_d} = \frac{D}{1 - D}}$$

- Assuming $P_d = P_o$

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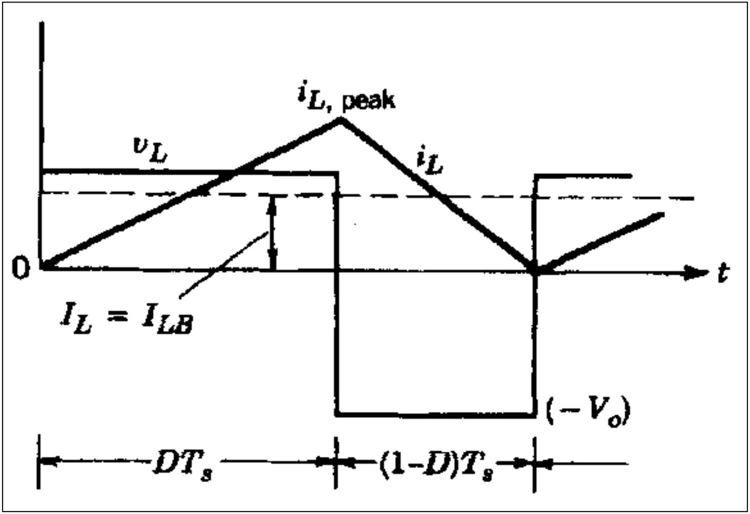
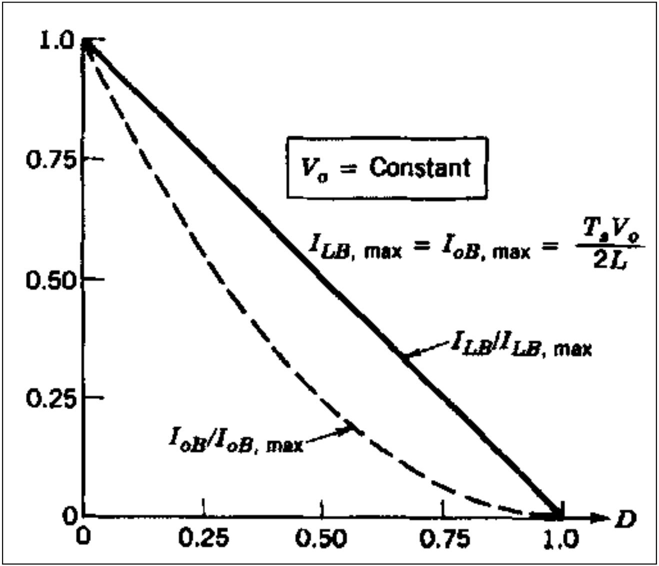
- Assuming $P_d = P_o$

$$\frac{I_o}{I_d} = \frac{1 - D}{D}$$

- i_L goes to zero at the end of OFF period



5.2 Boundary between CCM and DCM



5.2 Boundary between CCM and DCM

- Average inductor current at boundary

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$$I_{LB} = \frac{1}{2} i_{L,\text{peak}}$$
$$= \frac{T_s V_d}{2L} D$$

- Average output current

- Average inductor current at boundary

$$I_{LB} = \frac{1}{2} i_{L,\text{peak}}$$
$$= \frac{T_s V_d}{2L} D$$

- Average output current

$$I_o = I_L - I_d$$

- Average inductor current at boundary

$$I_{LB} = \frac{1}{2} i_{L,\text{peak}}$$

$$= \frac{T_s V_d}{2L} D$$

- Average output current

$$I_o = I_L - I_d$$

$$I_{LB} = \frac{T_s V_o}{2L}(1 - D)$$

$$I_{oB} = \frac{T_s V_o}{2L}(1 - D)^2$$

- I_{LB} and I_o result in their maximum values at D = 0

- I_{LB} and I_o result in their maximum values at D = 0

$$I_{LB,\max} = \frac{T_s V_o}{2L}$$

$$I_{oB,\max} = \frac{T_s V_o}{2L}$$

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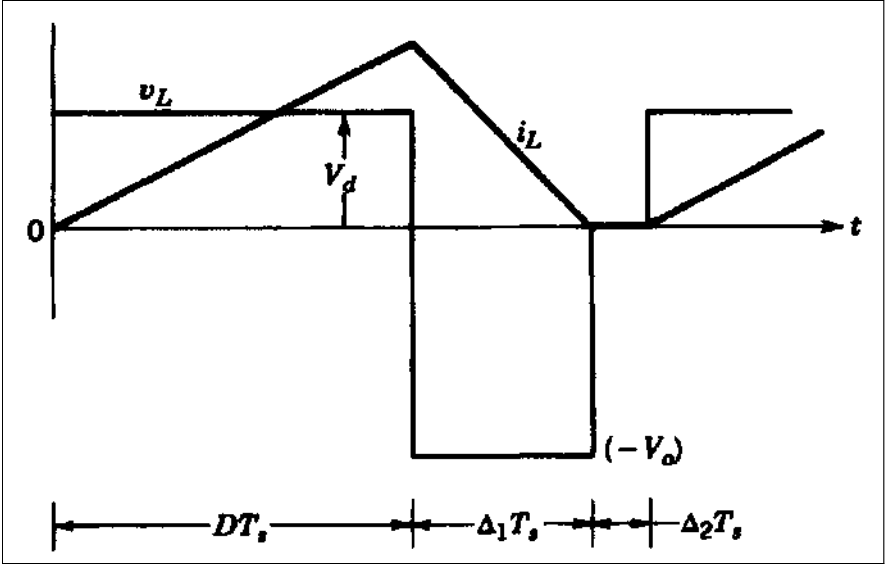
$$I_{oB,\max} = \frac{T_s V_o}{2L}$$

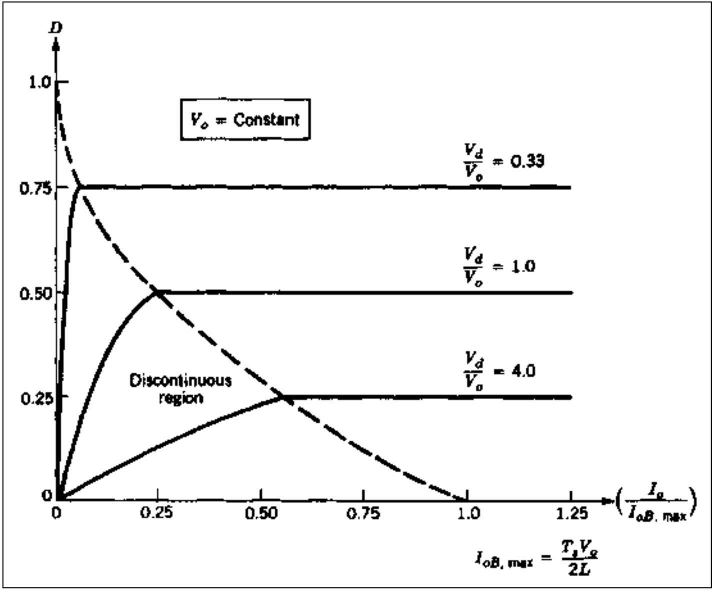
$$I_{LB} = I_{LB,\max}(1 - D)$$

$$I_{oB} = I_{oB,\max}(1 - D)^2$$

5.3 Discontinuous Conduction Mode



5.3 Discontinuous Conduction Mode



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$$V_d D T_s + (-V_o)\Delta_1 T_s = 0$$

$$\boxed{\frac{V_o}{V_d} = \frac{D}{\Delta_1}}$$

- Assuming $P_d = P_o$

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- Assuming $P_d = P_o$

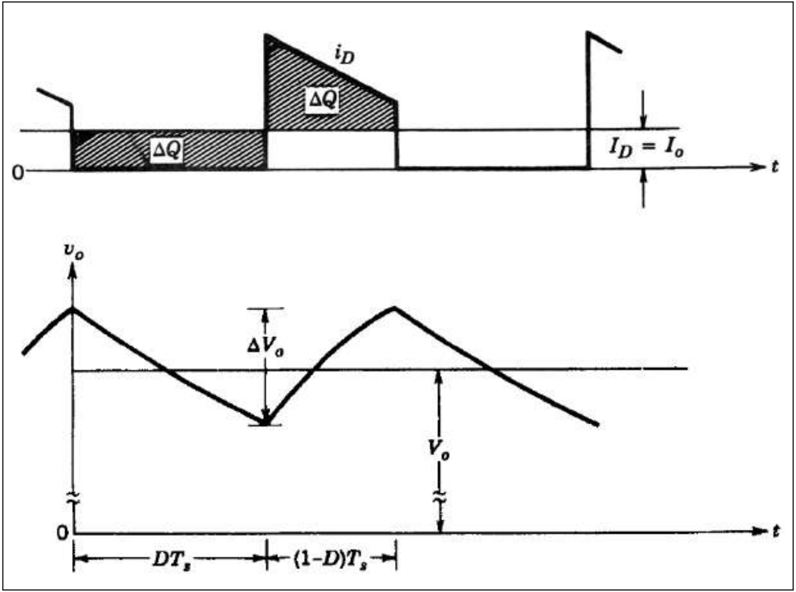
$$\frac{I_o}{I_d} = \frac{\Delta_1}{D}$$

$$I_L = \frac{V_d}{2L} DT_s(D + \Delta_1)$$

$$D = \frac{V_o}{V_d} \sqrt{\frac{I_o}{I_{oB,max}}}$$

- Boundary between the continuous mode and discontinuous mode is shown by the dashed curve.

5.4 Output Voltage Ripple



- Assuming that all the ripple current component of i_D flows through the capacitor and its average value flows through the load resistor, the shaded area represents charge ΔQ
- Peak to peak voltage ripple

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{I_o D T_s}{C}$$

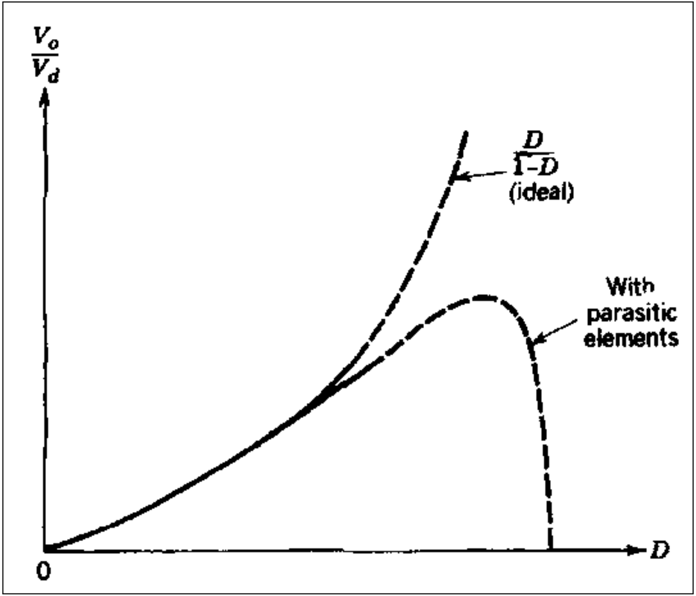
$$= \frac{V_o}{R}\frac{DT_s}{C}$$

$$\frac{\Delta V_o}{V_o} = \frac{DT_s}{RC}$$

$$= D\frac{T_s}{\tau}$$

where τ = RC is the time constant

5.5 Effect of Parasitic Elements



- Dashed curve shows very poor switch utilization, making very high duty ratios impractical
- Parasitic elements will affect the voltage conversion ratio and the stability of the feedback regulated buck-boost converter.

Problem

Q) In a buck-boost converter operating at 20 kHz, L = 0.05 mH. The output capacitor C is sufficiently large and $V_d = 15$ V. The output is to be regulated at 10 V and the converter is supplying a load of 10 W. Calculate the duty ratio D.

Problem

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$$\frac{D}{1-D} = \frac{10}{15} \Rightarrow D = 0.4$$

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$$I_{oB,\max} = \frac{0.05 \times 10}{2 \times 0.05} = 5 \text{ A}$$

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$$I_{oB} = 5(1-0.4)^2 = 1.8\ A$$

$$D = \frac{10}{15}\sqrt{\frac{1.0}{5.0}} = 0.3$$

References

1. Mohan, Undeland, Robbins, *"Power Electronics Converters Application and Design"*, Wiley-India
2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

*for private circulation only

Switched Mode Power Converters

(EE364)

S6-EEE

by

Prof. Dinto Mathew
Asst. Professor
Dept. of EEE, MACE

Module 2 - Overview

- Provides **negative polarity regulated output voltage** with respect to the common terminal of the input voltage
- $C_1 \rightarrow$ Storing and transferring energy from the input to the output
- In steady state, average inductor voltages V_{L1} & V_{L2} are zero

$$V_{C1} = V_d + V_o$$

- V_{C1} is larger than both V_d and V_o
- Large $C_1 \implies v_{C1} = V_{C1}$, even though it stores and transfers energy from the input to the output

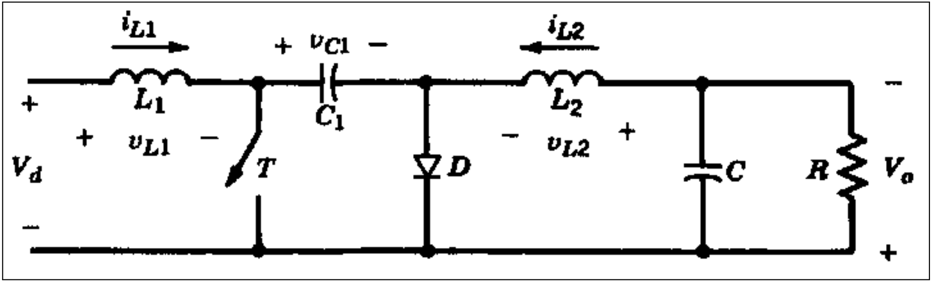
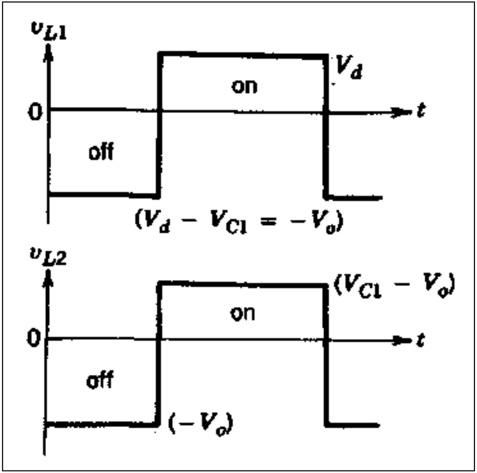
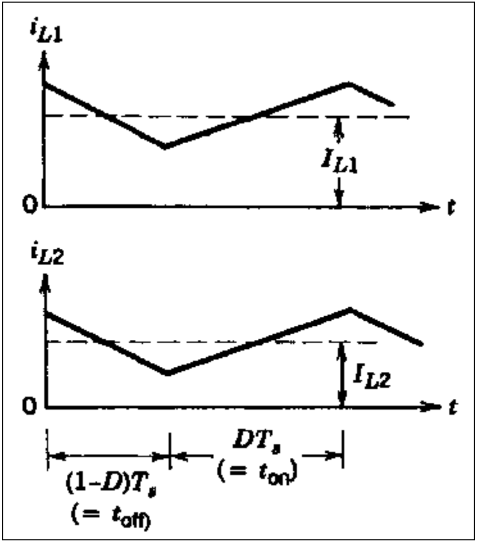


Figure 1 : Cuk Converter



v_{L1}
V_d
on
0
t
off
$(V_d - V_{C1} = -V_o)$
v_{L2}
$(V_{C1} - V_o)$
on
0
t
off
$(-V_o)$


i_{L1}
I_{L1}
0
t
i_{L2}
I_{L2}
0
t
DT_s
$(= t_{on})$
$(1-D)T_s$
$(= t_{off})$

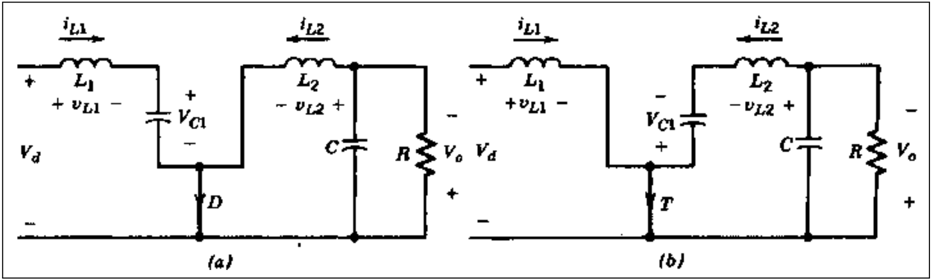


Figure 2 : Cuk Converter (a) Switch OFF (b) Switch ON

Operation

- When Switch is **OFF**
  - i_{L1} and i_{L2} flow through the diode
  - C_1 is charged through the diode by energy from both the input and L_1
  - i_{L1} decreases since $V_{C1} > V_d$
  - i_{L2} decreases since energy stored in L_2 feeds output

Operation

- When Switch is **OFF**
  - i_{L1} and i_{L2} flow through the diode
  - C_1 is charged through the diode by energy from both the input and L_1
  - i_{L1} decreases since $V_{C1} > V_d$
  - i_{L2} decreases since energy stored in L_2 feeds output
- When Switch is **ON**
  - V_{C1} reverse biases diode
  - i_{L1} & i_{L2} flow through the switch
  - C_1 discharges through the switch, transferring energy to the output and L_2 since $V_{C1} > V_o$
  - i_{L2} increases
  - Input feeds energy to L_1 causing i_{L1} to increase

1. Cuk Converter

- Let i_{L1} & i_{L2} are to be continuous $\implies$ **CCM**
- Assume V_{C1} to be constant
- Integral of v_{L1} & v_{L2} over one time period yields zero

1. Cuk Converter

- Let i_{L1} & i_{L2} are to be continuous $\implies$ **CCM**
- Assume V_{C1} to be constant
- Integral of v_{L1} & v_{L2} over one time period yields zero

$$V_d D T_s + (V_d - V_{C1})(1 - D)T_s = 0$$

$$V_{C1} = \frac{1}{1 - D} V_d$$

- Let i_{L1} & i_{L2} are to be continuous $\implies$ **CCM**
- Assume V_{C1} to be constant
- Integral of v_{L1} & v_{L2} over one time period yields zero

$$V_d DT_s + (V_d - V_{C1})(1 - D)T_s = 0$$

$$V_{C1} = \frac{1}{1 - D} V_d$$

$$(V_{C1} - V_o)DT_s + (-V_o)(1 - D)T_s = 0$$

$$V_{C1} = \frac{1}{D} V_o$$

- Let i_{L1} & i_{L2} are to be continuous $\implies$ **CCM**
- Assume V_{C1} to be constant
- Integral of v_{L1} & v_{L2} over one time period yields zero

$$V_d D T_s + (V_d - V_{C1})(1 - D)T_s = 0$$

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$$\boxed{\frac{V_o}{V_d} = \frac{D}{1 - D}}$$

1. Cuk Converter

- Assuming $P_d = P_o$

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$$\frac{I_o}{I_d} = \frac{1 - D}{D}$$

- $I_{L1} = I_d$ and $I_{L2} = I_o$

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$$\frac{I_o}{I_d} = \frac{1-D}{D}$$

- $I_{L1} = I_d$ and $I_{L2} = I_o$
- Assume that i_{L1} and i_{L2} are ripple free $\implies$ $i_{L1} = I_{L1}$ and $i_{L2} = I_{L2}$
- When switch is OFF, the charge delivered to C_1 equals $I_{L1}(1-D)T_s$
- When switch is ON, the capacitor discharges by an amount $I_{L2}DT_s$
- In steady state, the net change of charge associated with C_1 over one time period must be zero

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$$I_{L1}(1-D)T_s = I_{L2}DT_s$$

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- Both the input current and the current feeding the output stage are reasonably ripple free
- Possible to simultaneously eliminate the ripples in i_{L1} and i_{L2} completely, leading to lower external filtering requirements

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- Possible to simultaneously eliminate the ripples in i_{L1} and i_{L2} completely, leading to lower external filtering requirements

Disadvantages

- Requirement of a capacitor C_1 with a large ripple current carrying capability

Problem

Q) In a Cuk converter operating at 50 kHz, L_1=L_2=1mH and C_1=5μF. $V_d = 10$ V and the output V_o is regulated to be constant at 5 V. It is supplying 5W to a load. Assume ideal components. Calculate the percentage errors in assuming a constant voltage across C_1 or in assuming constant currents i_{L1} and i_{L2}.

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$$\frac{D}{1-D} = \frac{5}{10} \Rightarrow D = 0.333$$

$$\Delta i_{L1} = \frac{V_{C1} - V_d}{L_1}(1-D)T_s$$

$$= \frac{(15-10)}{10^{-3}}(1-0.333) \times 20 \times 10^{-6}$$

$$= 0.067\ A$$

Problem

$$\Delta i_{L2} = \frac{V_o}{L_2}(1 - D)T_s$$
$$= \frac{5}{10^{-3}}(1 - 0.333) \times 20 \times 10^{-6}$$
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$$\frac{\Delta i_{L2}}{I_{L2}} = \frac{0.067 \times 100}{1.0} = 6.7\%$$

Problem

(b)

$$\Delta V_{C1} = \frac{1}{C}\int_0^{(1-D)T_s} i_{L1}\, dt$$

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$$= 1.33\ V$$

$$\frac{\Delta V_{C1}}{V_{C1}} = \frac{1.33\times100}{15} = 8.87\%$$

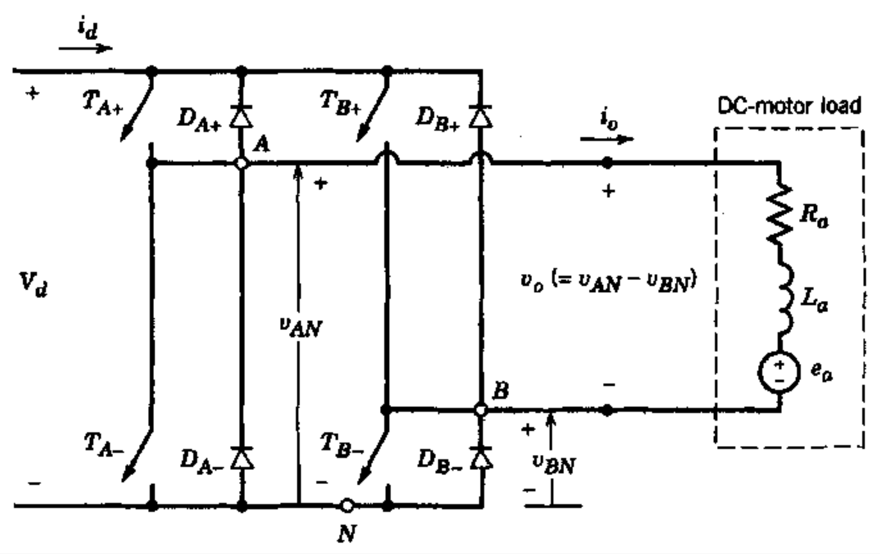
Applications

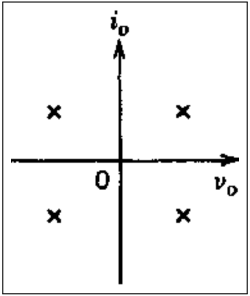
- **DC motor drives**
- Single phase uninterruptible AC power supplies
- Switch mode transformer isolated power supplies (DC to AC high/ intermediate frequency conversion)

Full Bridge DC-DC Converter

- Input is fixed magnitude DC voltage, V_d
- Output is DC voltage, V_o
- V_o can be controlled in **magnitude** as well as **polarity**
- **Magnitude** and **direction** of output current (i_o) can also be controlled
- Can operate in **all four quadrants** of ($i_o - v_o$) plane
- Power flow can be **in either direction**

2. Full Bridge DC-DC Converter





- Diodes are connected in antiparallel with switches
- **ON** state and **Conducting state** of switch
  - Since diodes are connected in antiparallel with the switches, when a switch is turned on, it may or may not conduct a current, depending on the direction of the output current
  - If switch conducts a current, then it is in a **conducting state**

2. Full Bridge DC-DC Converter

- Two legs, A and B
- Each leg consists of two switches and their antiparallel diodes
- The two switches in each leg are never OFF simultaneously
- In practice, they are both off for a short time interval, known as **blanking time**, to avoid short circuiting of DC input
- Output current, (i_o) will flow continuously

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Working

- If T_{A+} is ON and T_{A-} is OFF
  - i_o will flow through T_{A+} if i_o is positive OR
  - i_o will flow through D_{A+} if i_o is negative

$$v_{AN} = V_d$$

- If T_{A-} is ON and T_{A+} is OFF
  - i_o will flow through T_{A-} if i_o is negative OR
  - i_o will flow through D_{A-} if i_o is positive

$$v_{AN} = 0$$

- v_{AN} depends only on switch status and is **independent** of the direction of i_o

2. Full Bridge DC-DC Converter

- v_{AN} depends only on switch status and is **independent** of the direction of i_o
- V_{AN} (output voltage of converter leg A, averaged over one switching frequency time period, T_s) depends only on input voltage (V_d) and the duty ratio of T_{A+}

$$V_{AN} = \frac{V_d t_{\text{on}} + 0 \cdot t_{\text{off}}}{T_s} = V_d \cdot \text{duty ratio of } T_{A+}$$

- V_{BN}

$$V_{BN} = V_d \cdot \text{duty ratio of } T_{B+}$$

- Converter output voltage $V_o = V_{AN} - V_{BN}$
- V_o can be controlled by controlling the switch duty ratios and is independent of the magnitude and the direction of i_o

PWM Switching Strategies

1. PWM with Bipolar Voltage Switching
    - (T_{A+}, T_{B-}) and (T_{A-}, T_{B+}) are treated as two switch pairs
    - Switches in each pair are turned ON and OFF simultaneously

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2. PWM with Unipolar Voltage Switching (Double PWM Switching)
   - Switches in each inverter leg are controlled independently of the other leg

- In full bridge DC-DC converter for DC motor drives, input current (i_d) changes direction instantaneously. Hence it is important that the input to this converter be a **DC voltage source with a low internal impedance**. In practice, the large filter capacitor provides low impedance path to i_d

- Switches (T_{A+}, T_{B-}) and (T_{B+}, T_{A-}) are treated as two switch pairs
- Two switches in a pair are simultaneously turned ON and OFF)
- One of the two switch pairs is always on
- Switching signals are generated by comparing triangular waveform (v_{tri}) with control voltage $v_{control}$
    - When $v_{control} > v_{tri} \implies$ (T_{A+} and T_{B-}) are turned ON
    - When $v_{control} < v_{tri} \implies$ (T_{A-} and T_{B+}) are turned ON

$$v_{tri} = \hat{V}_{tri} \frac{t}{T_s/4} \qquad 0 < t < \tfrac{1}{4}T_s$$

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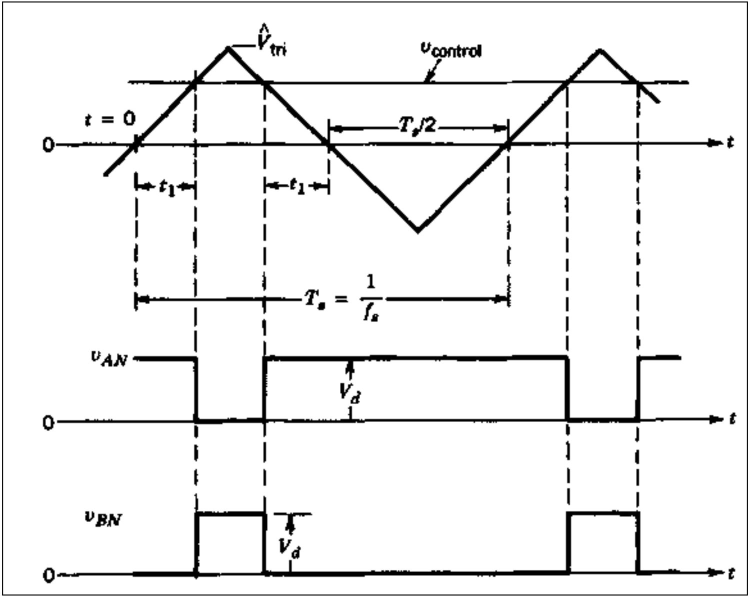
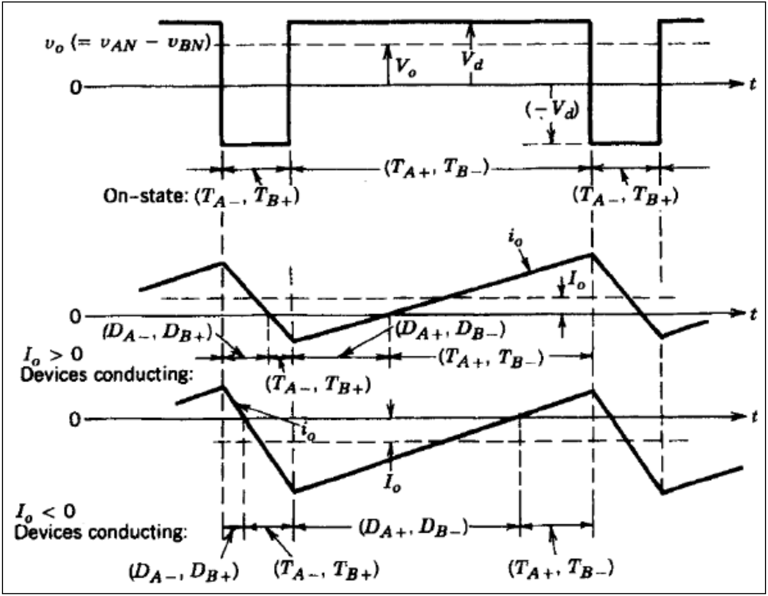
- At t $= t_1$, $v_{tri} = v_{control}$

$$t_1 = \frac{v_{control}}{\hat{V}_{tri}} \frac{T_s}{4}$$

2.1 PWM with Bipolar Voltage Switching





v_o (= $v_{AN} - v_{BN}$)
0
V_o
V_d
t
($-V_d$)
(T_{A+}, T_{B-})
On-state: (T_{A-}, T_{B+})
(T_{A-}, T_{B+})
i_o
I_o
0
t
(D_{A-}, D_{B+})
(D_{A+}, D_{B-})
$I_o > 0$
Devices conducting:
(T_{A+}, T_{B-})
(T_{A-}, T_{B+})
0
t
i_o
I_o
$I_o < 0$
Devices conducting:
(D_{A+}, D_{B-})
(D_{A-}, D_{B+})
(T_{A-}, T_{B+})
(T_{A+}, T_{B-})

2.1 PWM with Bipolar Voltage Switching

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$$t_{on} = 2t_1 + \frac{1}{2}T_s$$

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$$t_{\text{on}} = 2t_1 + \frac{1}{2}T_s$$

- Duty ratio of (T_{A+} and T_{B-})

$$D_1 = \frac{t_{\text{on}}}{T_s} = \frac{1}{2}\left(1 + \frac{v_{\text{control}}}{\hat{V}_{\text{tri}}}\right)$$

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- Duty ratio of (T_{A-} and T_{B+})

$$D_2 = 1 - D_1$$

$$V_o = V_{AN} - V_{BN} = D_1V_d - D_2V_d = (2D_1 - 1)V_d$$

$$V_o = \frac{V_d}{\hat{V}_{tri}} v_{control} = k v_{control}$$

- Average output voltage varies **linearly** with the input control signal

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- Blanking time introduces a slight non-linearity in the relationship between $v_{control}$ and V_o
- v_o switches between $+V_d$ and $-V_d$ $\implies$ **Bipolar Voltage Switching PWM**

2.1 PWM with Bipolar Voltage Switching

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- Average output voltage varies **linearly** with the input control signal
- Blanking time introduces a slight non-linearity in the relationship between $v_{control}$ and V_o
- v_o switches between $+V_d$ and $-V_d \implies$ **Bipolar Voltage Switching PWM**
- $0 < D_1 < 1 \implies -V_d < v_o < +V_d$
- v_o is independent of i_o since blanking time has been neglected
- Average output current (I_o), can be either positive or negative
  - For $I_o > 0$, $\rightarrow$ Average power flow is from V_d to V_o
  - For $I_o < 0$, $\rightarrow$ Average power flow is from V_o to V_d

2.2 PWM with Unipolar Voltage Switching

- Regardless of the direction of i_o,
  - $v_o = 0$ if T_{A+} and T_{B+} are both ON
  - $v_o = 0$ if T_{A-} and T_{B-} are both ON

- Regardless of the direction of i_o,
  - $v_o = 0$ if T_{A+} and T_{B+} are both ON
  - $v_o = 0$ if T_{A-} and T_{B-} are both ON
- Switching signal generation
  - Comparison of $v_{control}$ with v_{tri} controls leg A switches
  - Comparison of $-v_{control}$ with v_{tri} controls leg B switches

$$T_{A+} \text{ on:} \quad \text{if } v_{\text{control}} > v_{\text{tri}}$$

$$T_{B+} \text{ on:} \quad \text{if } -v_{\text{control}} > v_{\text{tri}}$$

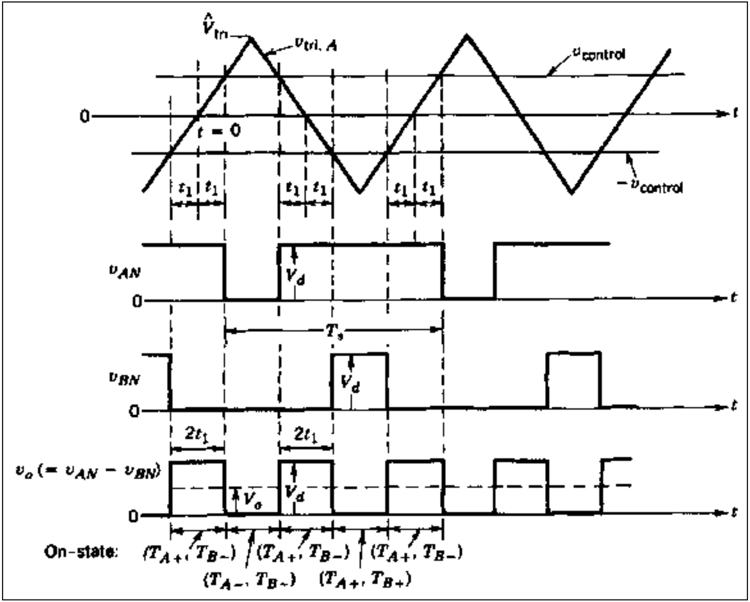
- Duty ratio of (T_{A+}, T_{B+})

$$D_1 = \frac{1}{2}\left(\frac{v_{\text{control}}}{\hat{V}_{\text{tri}}} + 1\right)$$

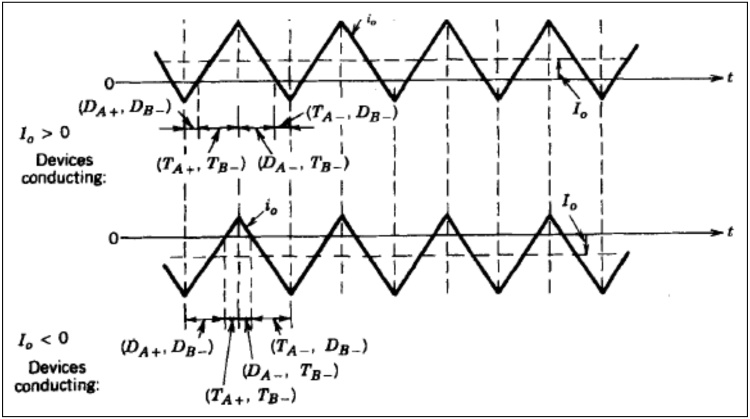
- Duty ratio of (T_{A-}, T_{B-})

$$D_2 = 1 - D_1$$

2.2 PWM with Unipolar Voltage Switching



2.2 PWM with Unipolar Voltage Switching



- Average output voltage V_o,

$$V_o = (2D_1 - 1)V_d = \frac{V_d}{\hat{V}_{\text{tri}}} v_{\text{control}}$$

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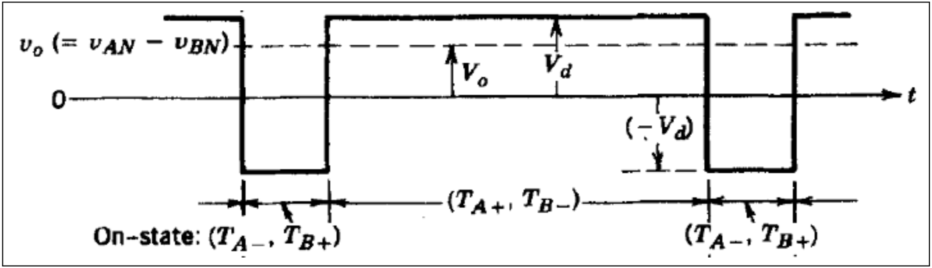
- Average output voltage (V_o) varies linearly with $v_{control}$
- V_o is positive in both modes
- If we consider same switching frequencies for bipolar and unipolar PWM strategies, then **unipolar voltage switching results in a better output voltage waveform** and in a better frequency response, since the effective switching frequency of the output voltage waveform is doubled and the ripple is reduced

Q) In a full bridge DC-DC converter, the input V_d, is constant and the output voltage is controlled by varying the duty ratio. Calculate the rms value of the ripple V_r, in the output voltage as a function of the average V_o, for

1. PWM with bipolar voltage switching
2. PWM with unipolar voltage switching

Ans : (1)



$$V_{o,\text{rms}} = V_d$$

$$V_o = V_{AN} - V_{BN} = D_1 V_d - D_2 V_d = (2D_1 - 1)V_d$$

$$V_{r,\text{rms}} = \sqrt{V_{o,\text{rms}}^2 - V_o^2} = V_d\sqrt{1 - (2D_1 - 1)^2} = 2V_d\sqrt{D_1 - D_1^2}$$

- As D_1 varies from 0 to 1, V_o varies from $-V_d$ to $+V_d$

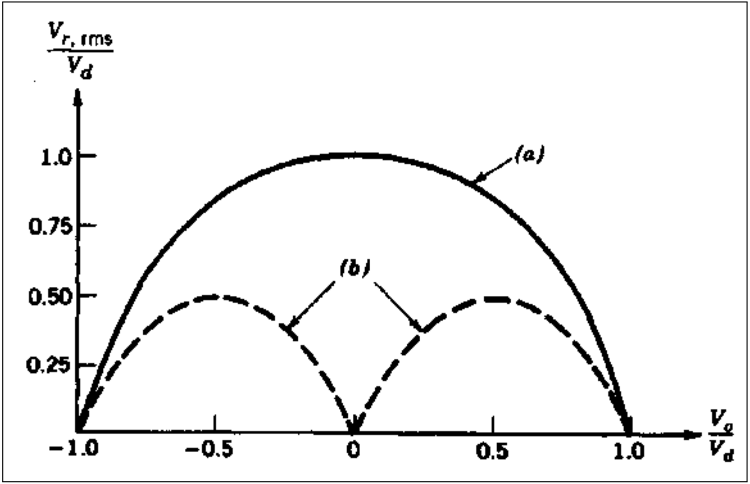
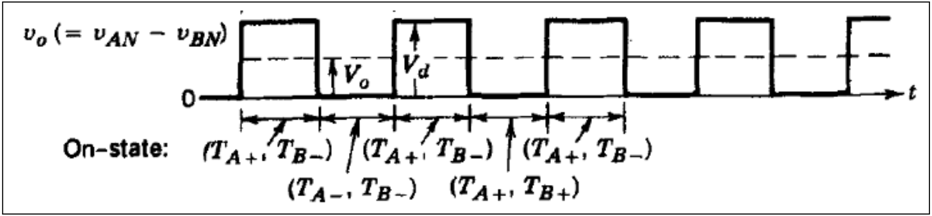


Figure 3 : V_{rms} in a full bridge converter using PWM (a) Bipolar voltage switching (b) Unipolar voltage switching

Ans : (2)



$$t_1 = \frac{v_{\text{control}}}{\hat{V}_{\text{tri}}} \frac{T_s}{4} \quad \text{for } v_{\text{control}} > 0$$

$$V_{o,\mathrm{rms}} = \sqrt{\frac{4t_1 V_d^2}{T_s}} = \sqrt{\frac{v_{\mathrm{control}}}{\hat{V}_{\mathrm{tri}}}}\, V_d = \sqrt{(2D_1 - 1)}V_d$$

$$V_{r,\mathrm{rms}} = \sqrt{V_{o,\mathrm{rms}}^2 - V_o^2} = \sqrt{6D_1 - 4D_1^2 - 2}V_d$$

- $v_{control} > 0$ and $0.5 < D < 1$
- As $v_{control}/V_{tri}$ varies from 0 to 1, D_1 varies from 0.5 to 1
- PWM with unipolar voltage switching results in a lower rms ripple component in the output voltage

3. Comparison of DC-DC Converters

- Buck, Boost, Buck-Boost and Cuk converters
  - Transfer energy only in one direction
  - Produce only unidirectional voltage and unidirectional current
- Full Bridge Converter
  - Bidirectional power flow
  - Both V_o and I_o can be reversed independently
  - Four quadrants ($V_o - I_o$ plane) operation $\rightarrow$ DC to AC Inverter

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Assumptions

- Average current is at its rated (designed maximum) value I_o
  - Ripple in the inductor current is negligible
  - $i_L = I_L$
  - Continuous Conduction Mode (CCM)
- Output voltage (v_o), is at its rated (designed maximum) value V_o
  - Ripple in v_o is negligible
  - $v_0 = V_o$
- Input voltage V_d is allowed to vary
  - Switch duty ratio must be controlled to hold V_o constant

- Switch peak voltage rating $= V_T$
- Switch peak current rating $= I_T$
- Switch power rating, $P_T = V_T \times I_T$
- Switch Utilization Factor $= \dfrac{P_o}{P_T}$

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- Switch power rating, $P_T = V_T \times I_T$
- Switch Utilization Factor $= \dfrac{P_o}{P_T}$
- In Buck and Boost converters, if the input and the output voltages are of the same order of magnitude, then the switch utilization factor is very good
- In Buck-Boost and Cuk converter, the switch utilization factor is poor
  - Maximum Switch Utilization Factor $= 0.25$ at D $= 0.5 \implies V_o = V_d$
- In non-isolated full bridge converter, overall switch utilization is very poor
  - Maximum Switch Utilization Factor occurs at $V_o = -V_d$ and $V_o = +V_d$ respectively

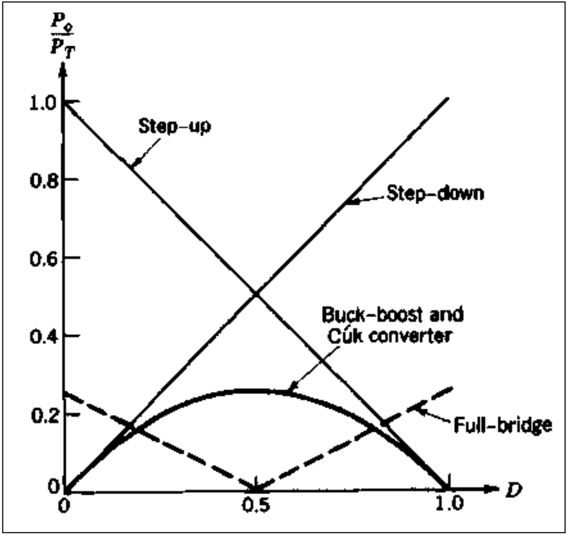

Figure 4 : Switch utilization in DC-DC converters

Conclusion

- Good switch utilization $\rightarrow$ either **Buck or Boost Converter**
- If both higher as well as lower output voltages compared to the input are necessary OR a negative polarity output compared to the input is desired $\rightarrow$ **Buck-Boost or Cuk Converter**
- Four quadrant operation $\rightarrow$ **Non-isolated Full Bridge Converter**

Converter Equivalent Circuits

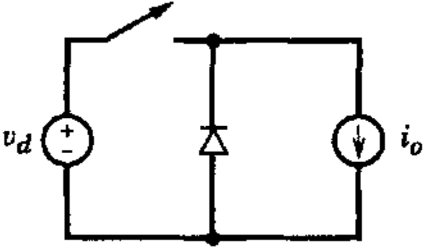

Figure 5 : Buck Converter

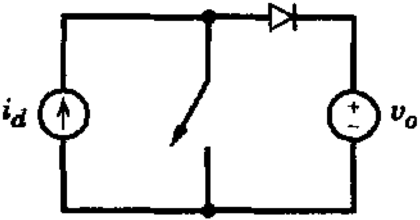

Figure 6 : Boost Converter

Converter Equivalent Circuits

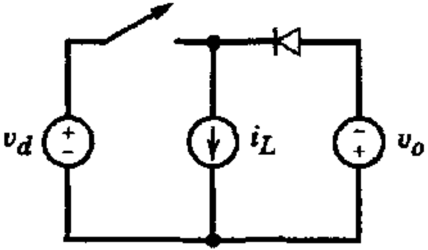

Figure 7 : Buck-Boost Converter

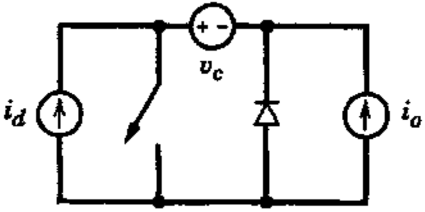

Figure 8 : Cuk Converter

Converter Equivalent Circuits

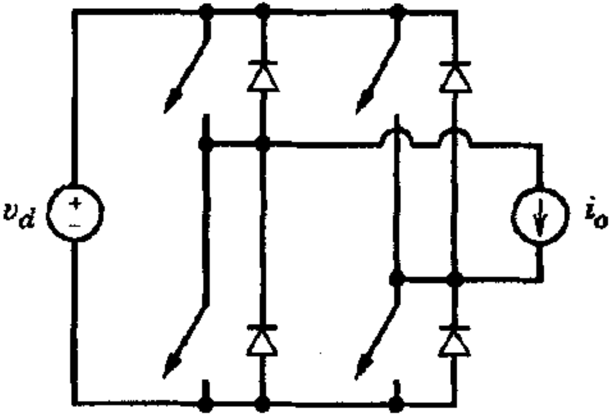

Figure 9 : Full Bridge Converter

Summary

- In any converter circuit operating in steady state
  - Capacitor can be represented by it's instantaneous voltage as an equivalent voltage source
  - Inductor can be represented by it's instantaneous current as an equivalent current source
- In all converters, the switching action does not cause discontinuity in the value of the voltage source or in the current source
- In **Buck (including full-bridge) and Boost converters**, the energy transfer is between a voltage and a current source
- In **Buck-Boost and Cuk converters**, the energy transfer is between two similar types of sources but they are separated by a source of the other type (eg: Buck-Boost Converter, two voltage sources are separated by a current source)

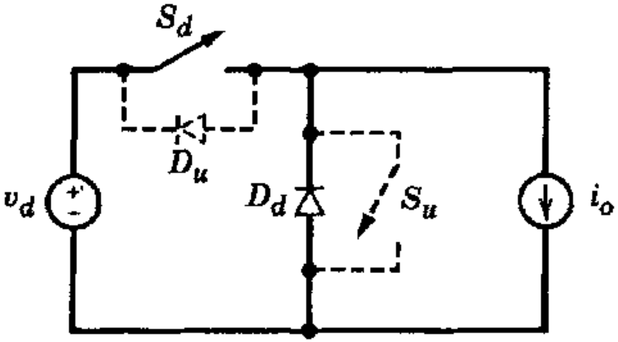

Figure 10 : Reversible power flow with reversible direction of the output current i_o

- Reversible power flow $\rightarrow$ Add additional diode and a switch
- Converter with a positive value of i_o and with S_d & D_d operating, resembles a **Buck Converter** where the flow of power is from the voltage source to the equivalent current source
- Converter with a negative value of i_o and with S_u & D_u operating, resembles a **Boost Converter** where the flow of power is from the equivalent current source to the voltage source

Regulated DC Power Supplies

- **Regulated Output**
  - V_o must be held constant within a specified tolerance for changes within a specified range in the input voltage and the output loading
- **Isolation**
  - Output may be electrically isolated from the input
- **Multiple Outputs**
  - Multiple outputs (positive and negative) that may differ in their voltage and current ratings
  - Multiple outputs may be isolated from each other

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  - Multiple outputs may be isolated from each other

- Reduce power supply size, weight & improve efficiency
- Power supplies
  - Linear Power Supplies
  - Switched Mode Power Supplies (smaller & much more efficient)

- To provide electrical isolation between the input and the output and to deliver the output in the desired voltage range, a 60 Hz transformer is needed
- Transistor operating in it's active region is connected in series
- By comparing V_o with V_{ref}, the control circuit adjusts the transistor base current such that V_o $(= v_d - v_{CE})$ equals $V_{o,ref}$
- Transistor acts as an adjustable resistor where the voltage difference $(v_d - V_o)$ appears across the transistor and causes power losses in it
- To minimize transistor power losses, the transformer turns ratio should be selected such that $V_{d,min} > V_o$, but does not exceed V_o by a large margin

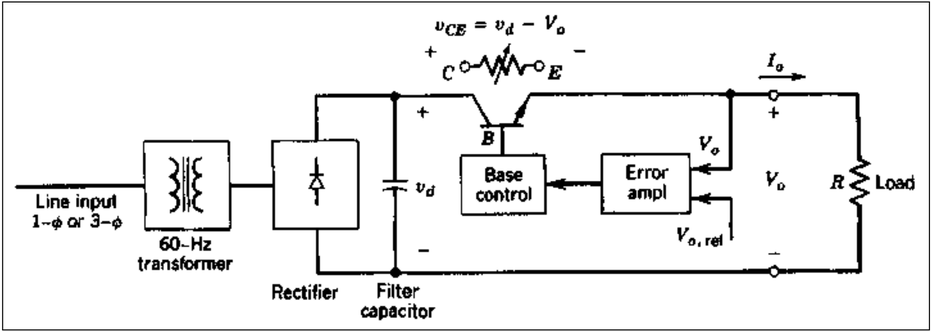


Figure 11 : Schematic of Linear Power Supply

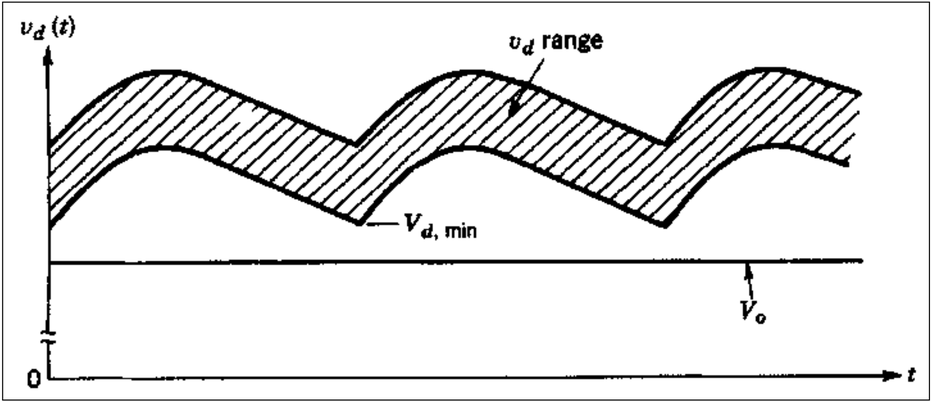


Figure 12 : Selection of Transformer Turns Ratio ($V_{d,min} > V_o$ by a small margin)

Advantages

- Utilize simple circuitry $\rightarrow$ Cost is less in small power ratings ($<$ 25 W)
- Do not produce large EMI with other equipment

4. Linear Power Supply

Advantages

- Utilize simple circuitry $\rightarrow$ Cost is less in small power ratings ($<$ 25 W)
- Do not produce large EMI with other equipment

Disadvantages

- A low frequency (60-Hz) transformer is required
  - Larger in size and weight compared to high-frequency transformers
- Transistor operates in it's active region, incurring a significant amount of power loss
  - Overall efficiency of linear power supplies is in a range of 30 - 60%

- Voltage transformation is accomplished by using DC to DC converter circuits
- Converter circuits use solid state devices (MOSFETs, IGBTs etc.), which operate as a switch $\rightarrow$ either **completely OFF** or **completely ON** $\implies$ Lower power dissipation
- Increased switching speeds, higher voltage & current ratings and relatively lower cost

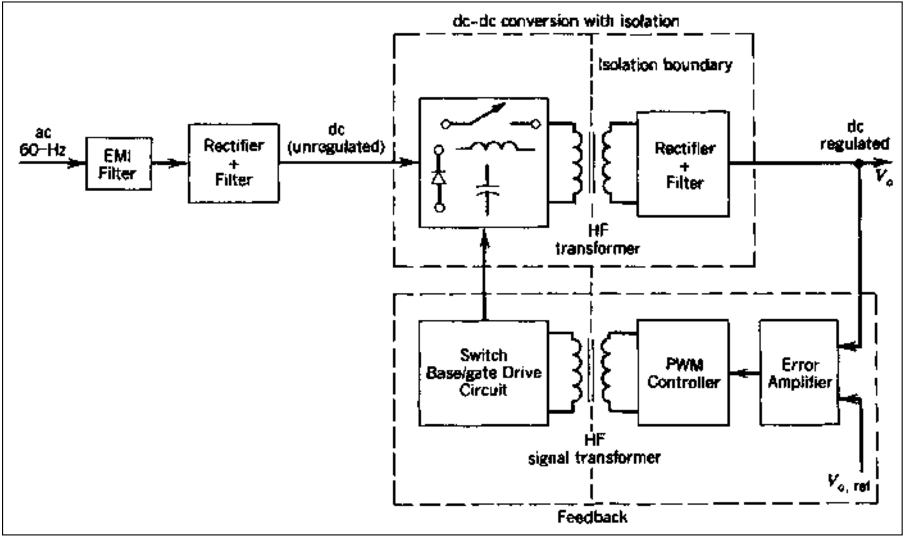
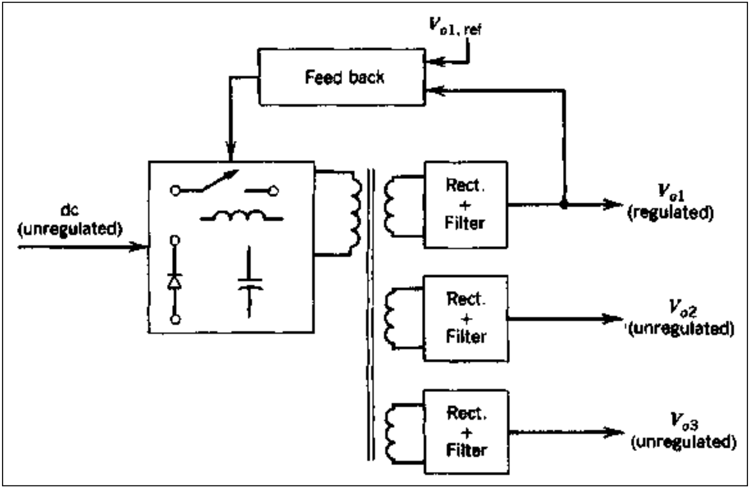


Figure 13 : Schematic of Switched Mode DC Power Supply

Working

- Input AC voltage is rectified into an unregulated DC voltage by diode rectifier
- EMI filter is used at the input to prevent the conducted EMI
- DC-DC converter converts input DC voltage from one level to another DC level $\rightarrow$ High frequency switching which produces high frequency AC across isolation transformer
- Secondary output of transformer is rectified and filtered to produce V_o
- V_o is regulated by feedback control that employs a PWM controller
- Electrical isolation in the feedback loop is provided either through an isolation transformer or through an optocoupler



- V_{o1} is regulated and the other two are unregulated
- If V_{o2} and/or V_{o3} needs to be regulated, linear regulator(s) can be used

5. Switched Mode Power Supply

Advantages of **Switched Mode Power Supply** over Linear Power Supply

- Switching elements (power transistors or MOSFETs) operate as a switch: either completely OFF or completely ON
  - Significant reduction in power losses
  - Higher energy efficiency in a 70 - 90% range
  - Larger power handling capability
- Size & weight of switching supplies can be significantly reduced due to the use of high frequency isolation transformer (as compared to a 50 or 60 Hz transformer in a linear power supply)

Advantages of **Switched Mode Power Supply** over Linear Power Supply

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  - Higher energy efficiency in a 70 - 90% range
  - Larger power handling capability
- Size & weight of switching supplies can be significantly reduced due to the use of high frequency isolation transformer (as compared to a 50 or 60 Hz transformer in a linear power supply)

Disadvantages

- Switching power supplies are more complex
- Proper measures must be taken to prevent EMI due to high frequency switchings

Switching DC Power Supplies

1. **Switched Mode DC-DC Converters**
   - Switches operate in a switch mode
2. **Resonant Converters**
   - Utilize Zero Voltage and/or Zero Current switchings

- High frequency isolation transformer provides electrical isolation
- Transformer Core Characteristics ie, **B-H (Hysteresis) Loop**
  - $B_m \rightarrow$ Maximum flux density beyond which saturation occurs
  - $B_r \rightarrow$ Remnant flux density

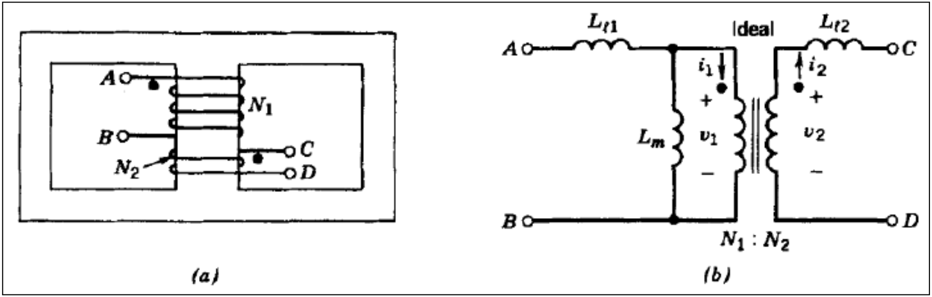

Figure 14 : (a) Two-winding transformer (b) Equivalent circuit

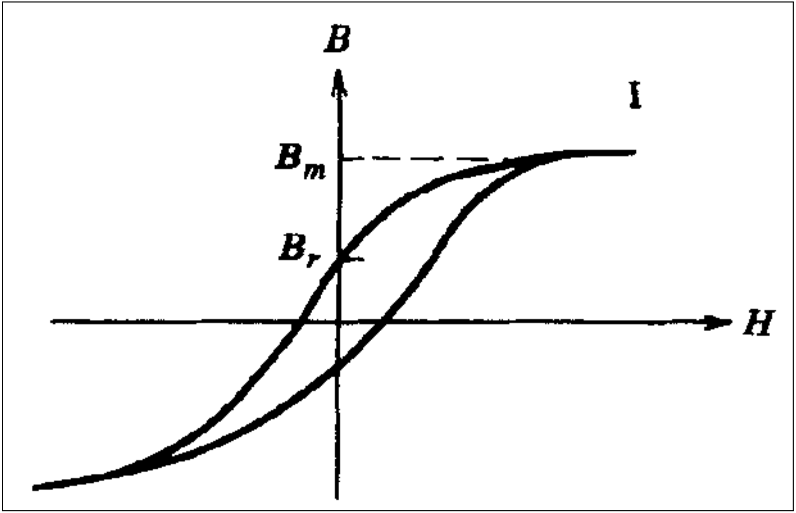

Figure 15 : Typical B-H loop of transformer core

Isolation Transformer Representation

- High frequency transformer provides electrical isolation
- $N_1 : N_2 =$ Transformer winding turns ratio
- $L_m =$ Magnetizing inductance referred to primary side
- L_{l1} & $L_{l2} =$ Leakage inductances
- For ideal transformer
  - $v_1/v_2 = N_1/N_2$
  - $N_1 i_1 = N_2 i_2$
- Leakage inductances (L_{l1} & L_{l2}) are minimized by providing a tight magnetic coupling between the two windings
- Magnetizing inductance (L_m) is made as high as possible to minimize the magnetizing current i_m, that flows through the switches $\rightarrow$ minimizes switch current ratings

Isolation Transformer Representation

- In Flyback Converter, the transformer provides
  - Energy storage as in an inductor
  - Electrical isolation as in a transformer
- In Resonant Converters
  - Leakage inductances and/or the magnetizing inductance may be utilized to provide zero-voltage and/or zero-current switchings

DC-DC Converters (with isolation) : based on the way how transformer core is utilized

1. **Unidirectional Core Excitation**
   - Only the positive part (quadrant 1) of the B-H loop is used
2. **Bidirectional Core excitation**
   - Both the positive (quadrant 1) and the negative (quadrant 3) parts of the B-H loop are utilized alternatively

- DC-DC converters with electrical isolation (provided by means of unidirectional core excitation)

Types

1. Flyback Converter (derived from Buck-Boost Converter)
2. Forward Converter (derived from Buck Converter)

- DC-DC converters with electrical isolation (provided by means of bidirectional core excitation)

Types

1. Push-Pull Converter
2. Half Bridge Converter
3. Full Bridge Converter

- In flyback and the forward converters, V_o is controlled by PWM
- In push-pull, half-bridge and full-bridge DC-DC converters, V_o is controlled by using PWM scheme which controls the interval A during which all the switches are OFF simultaneously

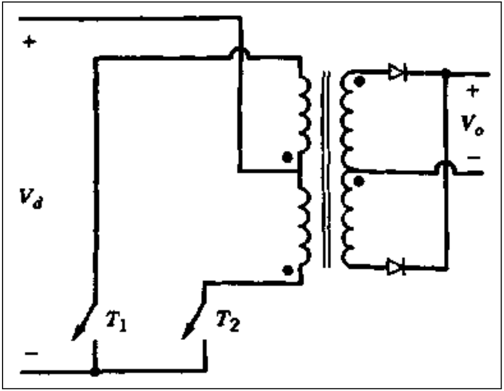

Figure 16 : Push-Pull Converter

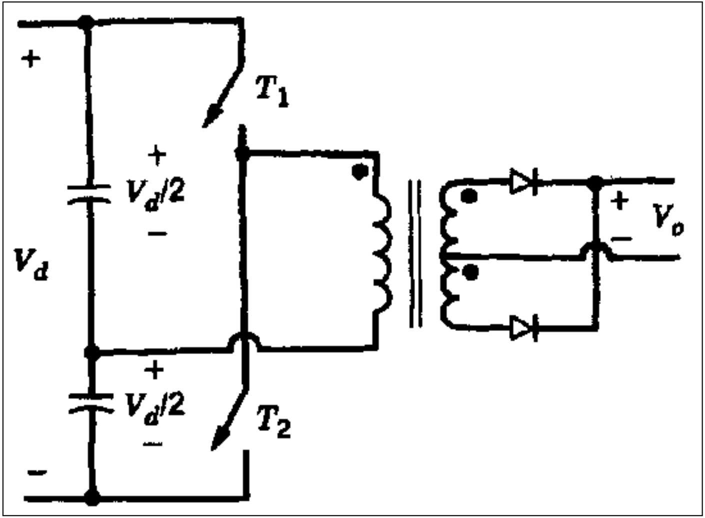

Figure 17 : Half Bridge Converter

Control of DC-DC Converters with Isolation

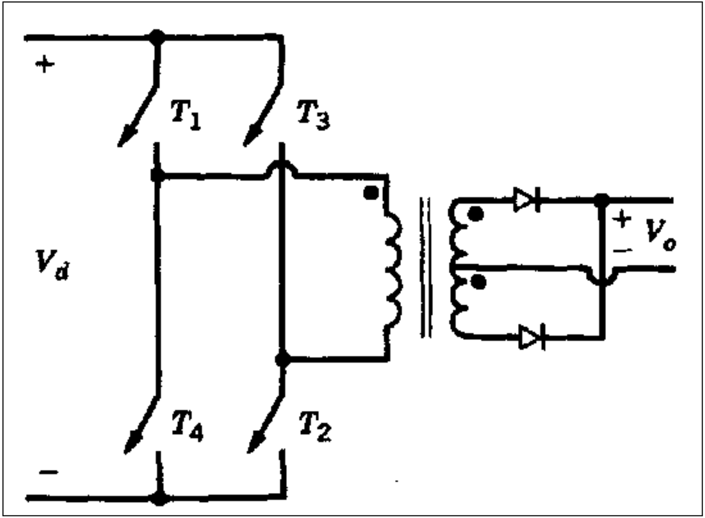

Figure 18 : Full Bridge Converter

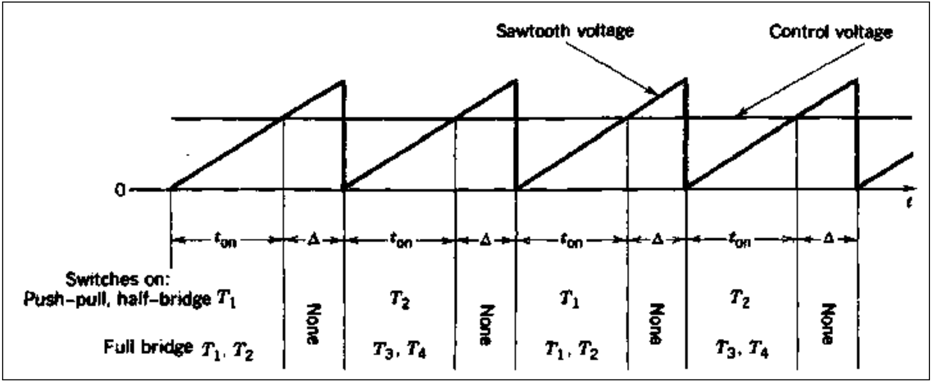

Figure 19 : PWM Scheme used in DC-DC converters

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1. Mohan, Undeland, Robbins, *"Power Electronics Converters Application and Design"*, Wiley-India
2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

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Switched Mode Power Converters

(EE364)

S6-EEE

by

Prof. Dinto Mathew
Asst. Professor
Dept. of EEE, MACE

Module 3 - Overview

- Derived from the Buck-Boost converter

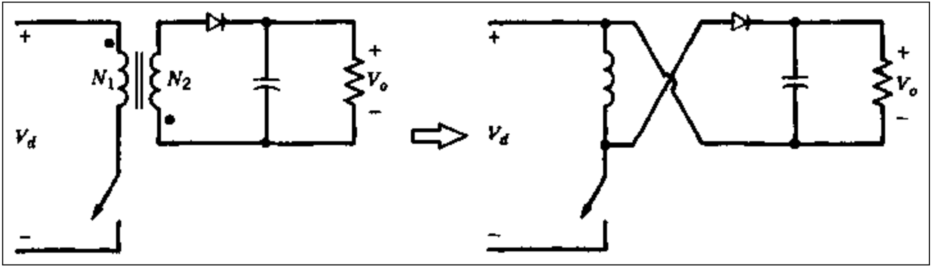


Figure 1 : Fly Back Converter derived from Buck-Boost Converter

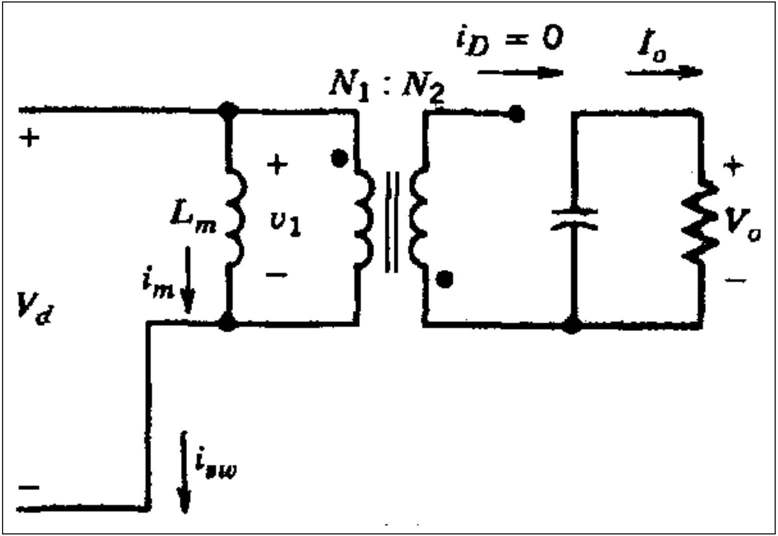


Figure 2 : Fly Back Converter with switch ON

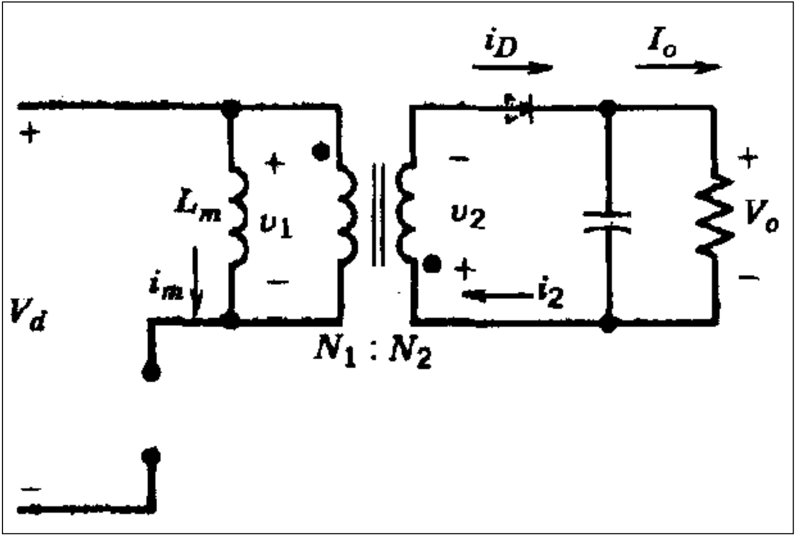
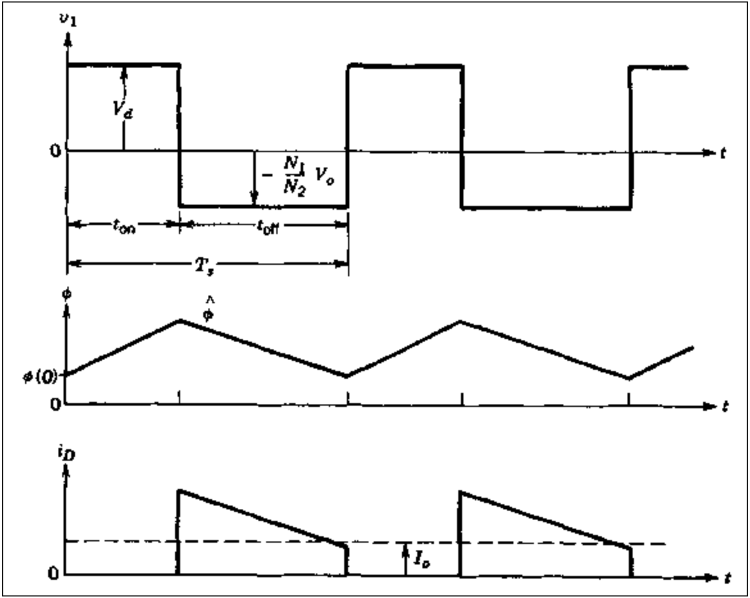


Figure 3 : Fly Back Converter with switch OFF

1.1 Continuous Conduction Mode



- <u>When switch is **ON**</u>
    - Diode (D) is reverse biased due to the winding polarities
    - Inductor core flux increases linearly from it's initial value $\Phi(0)$

$$\phi(t) = \phi(0) + \frac{V_d}{N_1}t \qquad 0 < t < t_{on}$$

- When switch is **ON**
  - Diode (D) is reverse biased due to the winding polarities
  - Inductor core flux increases linearly from it's initial value $\Phi(0)$

$$\phi(t) = \phi(0) + \frac{V_d}{N_1}t \qquad 0 < t < t_{on}$$

  - Peak flux at the end of ON interval

$$\hat{\phi} = \phi(t_{on}) = \phi(0) + \frac{V_d}{N_1}t_{on}$$

- <u>When switch is **OFF**</u>
  - Diode D is forward biased
  - Energy stored in the core causes the current to flow in the secondary winding through the diode
  - Voltage across the secondary winding $v_2 = -V_0 \implies$ Flux decreases linearly

$$\phi(t) = \hat{\phi} - \frac{V_o}{N_2}(t - t_{on}) \qquad t_{on} < t < T_s$$

$$\begin{aligned} \phi(T_s) &= \hat{\phi} - \frac{V_o}{N_2}(T_s - t_{on}) \\ &= \phi(0) + \frac{V_d}{N_1}t_{on} - \frac{V_o}{N_2}(T_s - t_{on}) \end{aligned}$$

- Net change of flux through the core over one time period must be zero in steady state $\Longrightarrow$

$$\phi(T_s) = \phi(0)$$

$$\boxed{\frac{V_o}{V_d} = \frac{N_2}{N_1}\frac{D}{1-D}}$$

- Voltage transfer ratio depends on D in an identical manner as the Buck-Boost converter
- During ON interval, the transformer primary voltage $v_1 = +V_d \Longrightarrow$ Inductor current rises linearly from it's initial value $I_m(0)$

$$i_m(t) = i_{sw}(t) = I_m(0) + \frac{V_d}{L_m}t \qquad 0 < t < t_{on}$$

$$\hat{I}_m = \hat{I}_{sw} = I_m(0) + \frac{V_d}{L_m} t_{on}$$

- During OFF interval
    - Switch current goes to zero
    - $v_1 = -(N_1/N_2)V_o$

$$\hat{I}_m = \hat{I}_{sw} = I_m(0) + \frac{V_d}{L_m} t_{on}$$

- During OFF interval
  - Switch current goes to zero
  - $v_1 = -(N_1/N_2)V_o$
- During $t_{on} < t < T_s$

$$i_m(t) = \hat{I}_m - \frac{V_o(N_1/N_2)}{L_m}(t - t_{on})$$

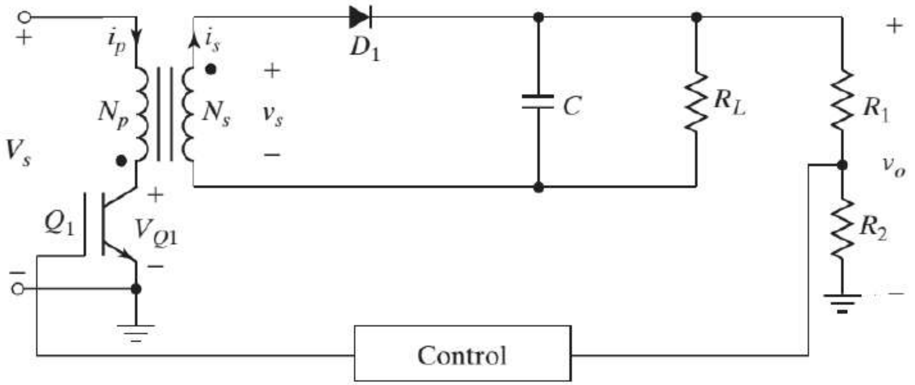
$$i_D(t) = \frac{N_1}{N_2} i_m(t) = \frac{N_1}{N_2}\left[\hat{I}_m - \frac{V_o(N_1/N_2)}{L_m}(t - t_{on})\right]$$

- Average diode current (I_0)

$$\hat{I}_m = \hat{I}_{sw} = \frac{N_2}{N_1}\frac{1}{1-D}I_o + \frac{N_1}{N_2}\frac{(1-D)T_s}{2L_m}V_o$$

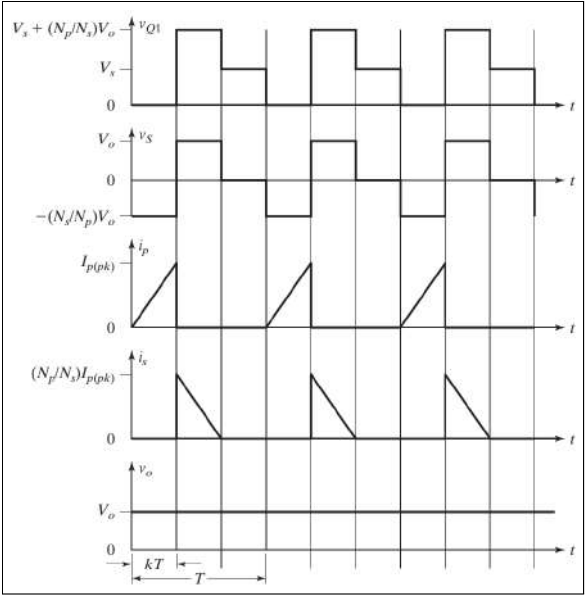
- Voltage across switch during the OFF interval

$$v_{sw} = V_d + \frac{N_1}{N_2}V_o = \frac{V_d}{1-D}$$



+
i_p
i_s
D_1
+
N_p
N_s
v_s
−
V_s
C
R_L
R_1
+
v_o
R_2
−
Q_1
+
V_{Q1}
−
−
Control

1.2 Discontinuous Conduction Mode



Mode 1 : When switch Q_1 is turned ON

- Mode 1 : $0 < t \leq kT$
  - k = Duty ratio
  - T = Switching period
- Voltage across primary winding of transformer = V_s
- D_1 is reverse biased
- No energy is transferred from input to load (R_L)
- Filter capacitor (C) maintains the output voltage and supplies the load current (i_L)
- i_p starts to build up & stores energy in primary winding

$$i_p = \frac{V_s t}{L_p}$$

  - L_p = Primary magnetizing inductance

At the end of Mode 1, at t = kT

- Primary current reaches peak value, $I_{p(pk)}$

$$I_{p(pk)} = i_p(t = kT) = \frac{V_s kT}{L_p}$$

- Peak secondary current, $I_{se(pk)}$

$$I_{se(pk)} = \left(\frac{N_p}{N_s}\right) I_{p(pk)}$$

Mode 2 : When switch Q_1 is turned OFF

- Polarity of the windings reverses due to the fact that i_p cannot change instantaneously
- D1 turns ON
- Output capacitor (C) charges
- Secondary current decreases linearly

$$i_{se} = I_{se(pk)} - \frac{V_o}{L_s}\, t$$

  - L_s = Secondary magnetizing inductance

- In discontinuous mode (DCM) operation, i_{se} decreases linearly to zero before the start of the next cycle

- Energy is transferred from the source to the output during the time interval 0 to kT only
- Input power (P_i)

$$P_i = \frac{\frac{1}{2} L_p I_{p(pk)}^2}{T} = \frac{(kV_s)^2}{2fL_p}$$

- Output power (P_o)

$$P_o = \eta P_i = \frac{\eta (V_s k)^2}{2fL_p}$$

$$P_o = V_o^2 / R_L$$

- Output voltage (V_o)

$$V_o = V_s k \sqrt{\frac{\eta R_L}{2fL_p}}$$

- V_o can be maintained constant by keeping the product $V_s kT$ constant
- k_{max} occurs at minimum supply voltage, $V_{s(min)}$

$$k_{\max} = \frac{V_o}{V_{s(\min)}}\sqrt{\frac{2fL_p}{\eta R_L}}$$

- V_o at k_{max}

$$V_o = V_{s(\min)} k_{\max}\sqrt{\frac{\eta R_L}{2fL_p}}$$

- Collector voltage V_{Q1} of Q_1 is maximum when V_s is maximum

$$V_{Q1(\max)} = V_{s(\max)} + \left(\frac{N_p}{N_s}\right) V_o$$

- Peak primary current, $I_{p(pk)}$ is same as maximum collector current

$$I_{C(\max)} = I_{p(pk)} = \frac{2P_i}{kV_s} = \frac{2P_o}{\eta V_s k}$$

- Flyback converter is used mostly in applications below 100 W
- Applications with high-output voltage at relatively low power
- Simple and low cost
- Switching device must be capable of sustaining a voltage $V_{Q1(max)}$

Continuous versus Discontinuous Mode of Operation

- In CCM, switch Q_1 is turned on before the secondary current falls to zero
  - CCM can provide higher power capability for the same value of peak current $I_{p(pk)}$
  - For the same output power, the peak currents in the DCM are much higher than those in CCM $\Longrightarrow$ A more expensive power transistor with a higher current rating is needed
  - Higher secondary peak currents in the DCM can have a larger transient spike at the instant of turn-off
- Still DCM is more preferred than the continuous mode
  - Inherently smaller magnetizing inductance in the discontinuous mode has a quicker response and a lower transient output voltage spike to sudden change in load current or input voltage.
  - CCM has a right-half-plane zero in it's transfer function, thereby making the feedback control circuit more difficult to design

Q) The average DC output voltage of the flyback circuit is $V_o = 24$ V at a resistive load of R = 0.8 Ω. The duty-cycle ratio is k = 50% and the switching frequency is f = 1 kHz. The on-state voltage drops of transistors and diodes are $V_t = 1.2$ V and $V_d = 0.7$ V respectively. The turns ratio of the transformer is a = $N_s/N_p = 0.25$. Determine
(a) Average input current I_s
(b)Efficiency η
(c) Average transistor current I_A
(d) Peak transistor current I_p
(e) RMS transistor current I_R
(f) Open-circuit transistor voltage V_{oc}
(g) Primary magnetizing inductor L_p
Neglect the losses in the transformer and the ripple current of the load.

$a = N_s/N_p = 0.25$ and $I_o = V_o/R = 24/0.8 = 30$ A.

a. The output power $P_o = V_o I_o = 24 \times 30 = 720$ W. The secondary voltage $V_2 = V_o + V_d = 24 + 0.7 = 24.7$ V. The primary voltage $V_1 = V_2/a = 24.7/0.25 = 98.8$ V. The input voltage $V_s = V_1 + V_t = 98.8 + 1.2 = 100$ and the input power is

$$P_i = V_s I_s = 1.2 I_A + V_d I_o + P_o$$

Substituting $I_A = I_s$ gives

$$I_s(100 - 1.2) = 0.7 \times 30 + 720$$

$$I_s = \frac{741}{98.8} = 7.5 \text{ A}$$

b. $P_i = V_s I_s = 100 \times 7.5 = 750$ W. The efficiency $\eta = 7.5/750 = 96.0\%$.

c. $I_A = I_s = 7.5$ A.

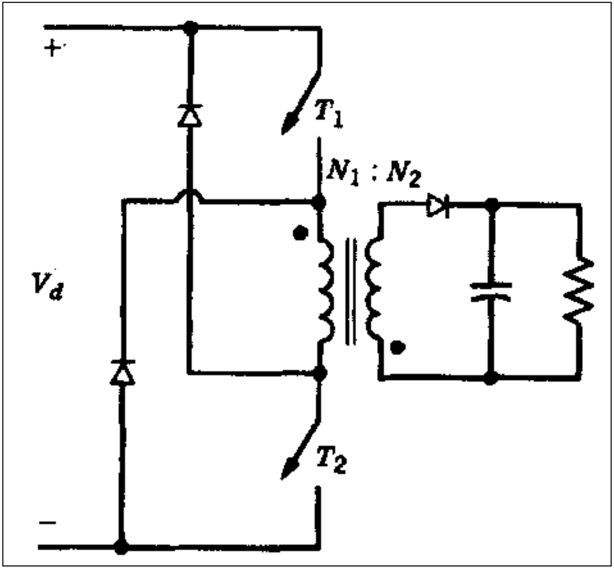
d. $I_p = 2I_A/k = 2 \times 7.5/0.5 = 30$ A.

e. $I_R = \sqrt{k/3} I_p = \sqrt{0.5/3} \times 30 = 12.25$ A, for 50% duty cycle.

f. $V_{oc} = V_s + V_2/a = 100 + 24.7/0.25 = 198.8$ V.

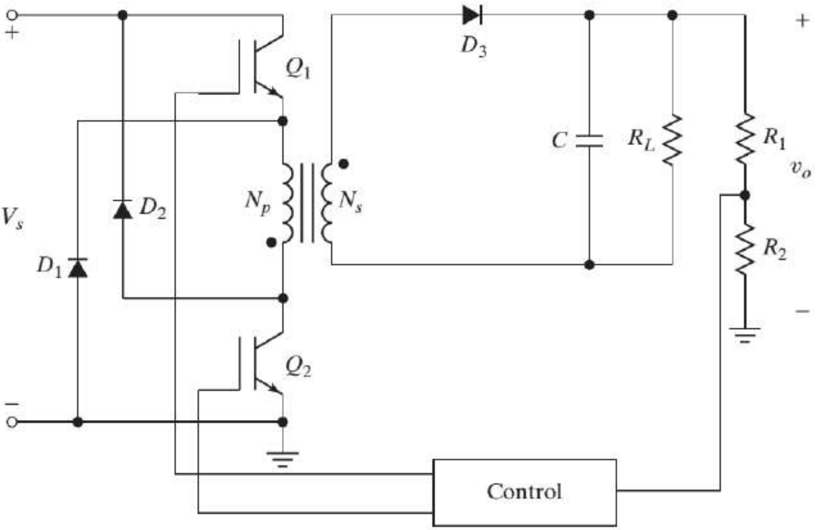
g. Using Eq. (13.2) for I_p gives $L_p = V_s k/f I_p = 100 \times 0.5/(1 \times 10^{-3} \times 30) = 1.67$ mH.

2. Double Ended Fly Back Converter

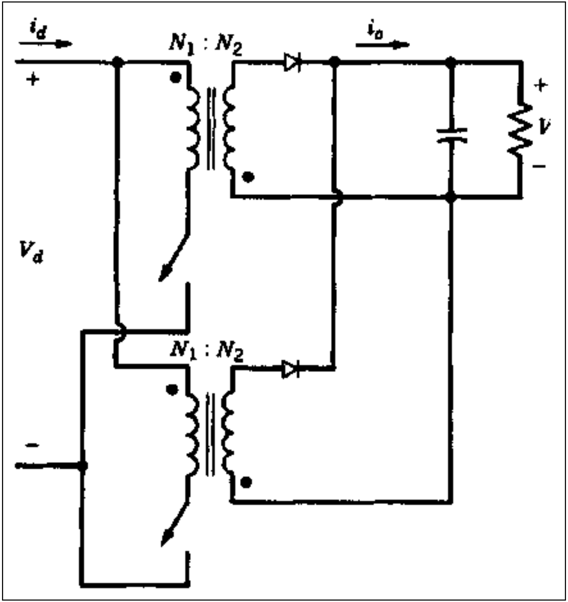


- **Two-Transistor Flyback Converter**
- For relatively high-output voltage at low power applications
- T_1 and T_2 are turned ON and OFF simultaneously
- Diodes are used to limit the maximum switch voltage to V_d
- Advantages
  - Voltage rating of switches is one-half of the single-transistor fly back converter topology
  - Dissipative snubber across the primary winding is not needed to dissipate the energy associated with the transformer primary-winding leakage inductar since a current path exists through the diodes connected to the primary winding

2. Double Ended Fly Back Converter



Paralleling Flyback Converters



Paralleling Flyback Converters

- Both operate at the same switching frequency
  - Switches in the two converters are sequenced to turn ON a half-time period apart from one another $\rightarrow$ Improved input and output current waveforms
- Current sharing among the parallel converters can be controlled by means of current-mode control
- Advantages
  - Provides higher system reliability due to redundancy
  - Increases the effective switching frequency $\rightarrow$ Decreases current pulsations at the input and/or the output
  - Allows low power modules to be standardized where a number of these can be paralleled to provide a higher power capability

- Derived from Step-down (Buck) Converter
- Transformer magnetizing current must be considered
- Assuming transformer to be ideal, when the switch is ON
  - D_1 becomes forward biased and D_2 reverse biased

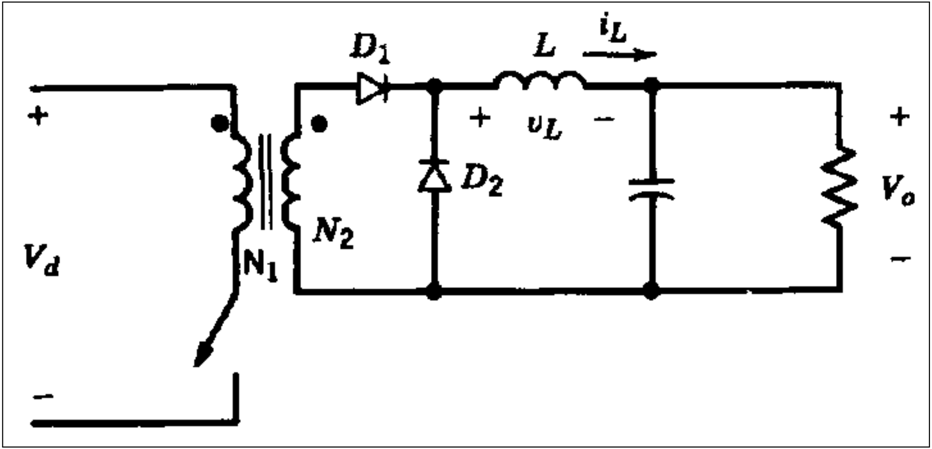
$$v_L = \frac{N_2}{N_1}V_d - V_o \qquad 0 < t < t_{on}$$

  - v_L is positive $\rightarrow$ i_L increases linearly
- When switch is turned OFF
  - D_2 is forward biased
  - inductor current i_L circulates through the diode D_2

$$v_L = -V_o \qquad t_{on} < t < T_s$$

  - v_L is negative $\rightarrow$ i_L decreases linearly

- **Idealized Forward Converter**



- Integral of inductor voltage over one time period is zero

$$\boxed{\frac{V_o}{V_d} = \frac{N_2}{N_1} D}$$

- Voltage rat
- Voltage ratio in the forward converter is proportional to the switch duty ratio D, similar to the step-down converter

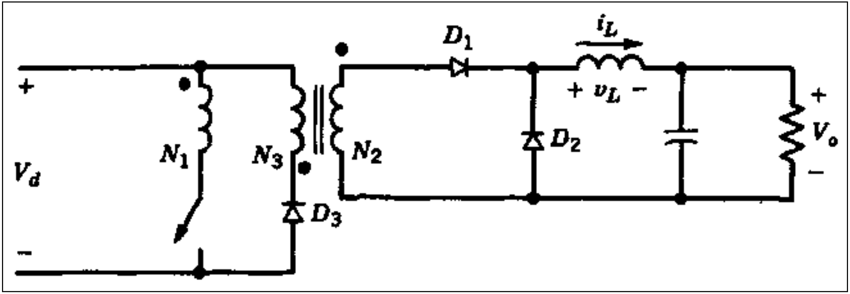
- Transformer magnetizing current must be taken into consideration. Otherwise, the stored energy in the transformer core would result in converter failure
- Practical approach that allows the transformer magnetic energy to be recovered and fed back to the input supply $\rightarrow$ **Demagnetizing winding**
- When switch is turned ON
  - i_m increases linearly from zero to $\hat{I_m}$

$$v_1 = V_d \qquad 0 < t < t_{on}$$

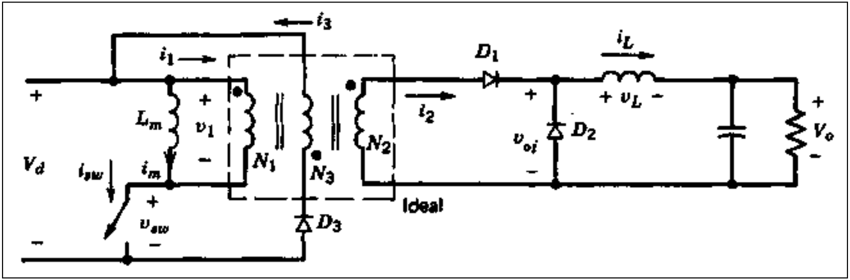
- When switch is turned OFF
  - $i_1 = -i_m$
  - $N_1 i_1 + N_3 i_3 = N_2 i_2$
  - D_1 is reverse biased $\implies$ $i_2 = 0$

$$i_3 = \frac{N_1}{N_3} i_m$$

  - i_3 flows through D_3 into the input DC supply

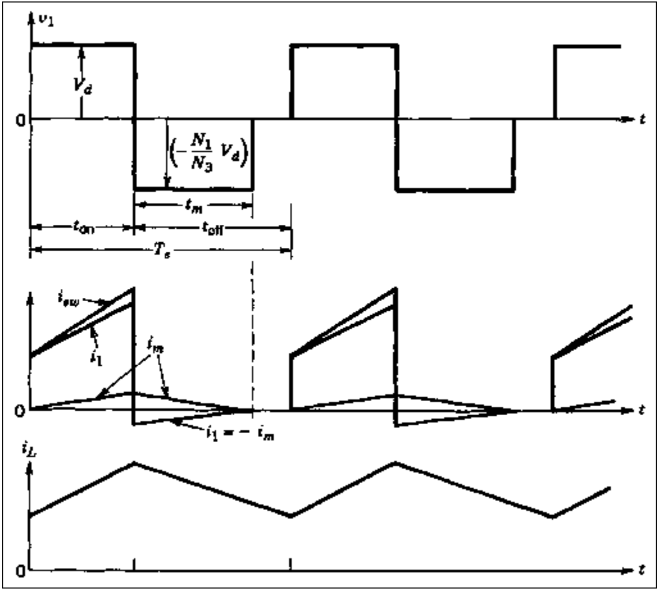


D_1
i_L
+
v_L
−
V_d
N_1
N_3
N_2
D_2
D_3
V_o



i_3
i_1
D_1
i_L
L_m
v_1
V_d
i_{sw}
i_m
v_{sw}
N_1
N_3
N_2
i_2
v_{oi}
D_2
D_3
v_L
V_o
Ideal

3.2 Practical Forward Converter



- During the time interval t_m,

$$v_1 = -\frac{N_1}{N_3}V_d \qquad t_{on} < t < t_{on} + t_m$$

- Once the transformer demagnetizes, $i_m = 0$ and $v_1 = 0$
- Time integral of voltage v_1 across L_m must be zero over one time period

$$\frac{t_m}{T_s} = \frac{N_3}{N_1}D$$

- If the transformer is to be totally demagnetized before the next cycle begins, the maximum value (t_m/T_s), can attain is (1 - D)
- Maximum duty ratio D, with a given turns ratio N_3/N_1

$$(1 - D_{max}) = \frac{N_3}{N_1}D_{max}$$

$$D_{max} = \frac{1}{1 + N_3/N_1}$$

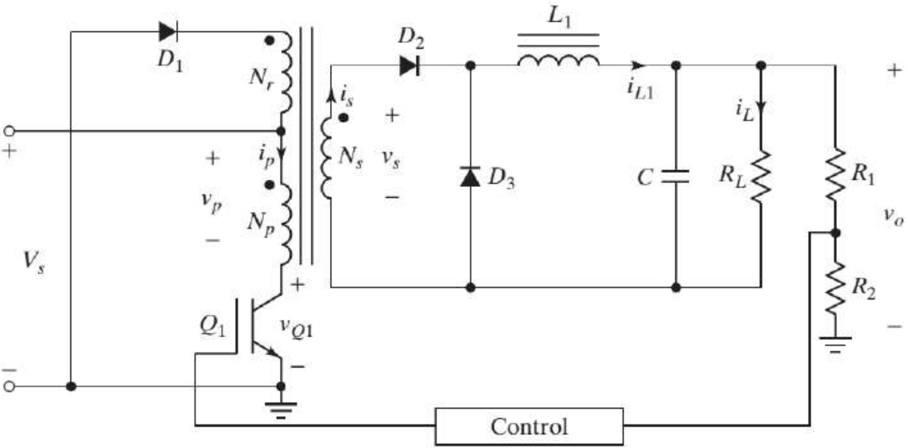
3.2 Practical Forward Converter

- With an equal number of turns for the primary and the demagnetizing windings ($N_1 = N_3$), the maximum duty ratio is limited to 0.5
- Since a large voltage isolation requirement does not exist between the primary and the demagnetizing windings, these two can be wound bifilar, in order to minimize the leakage inductance between the two windings
- Demagnetizing winding requires a much smaller size of wire, since it has to carry only the demagnetizing current
- Instead of using a third demagnetizing winding, the energy in the core can be dissipated in the Zener diode connected across the switch

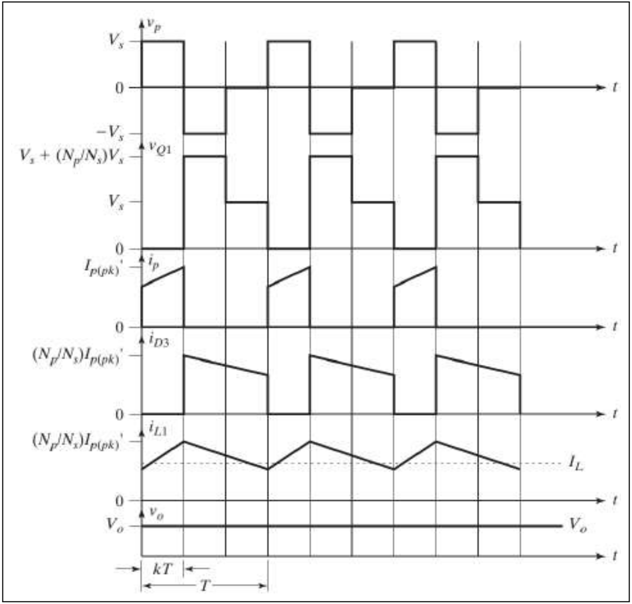
Forward Converter

- Transformer core is reset by reset winding
- Energy stored in the transformer core is returned to the supply $\Longrightarrow$ Efficiency is increased
- D_2 is forward biased when the voltage across the primary is positive. ie, when the transistor is ON
- Forward converter is operated in the continuous mode. In the discontinuous mode, the forward converter is more difficult to control because of a double pole existing at the output filter
- Operation
  - Mode 1 : When switch Q_1 is turned ON
  - Mode 2 : When switch Q_1 is turned OFF

Forward Converter



Forward Converters



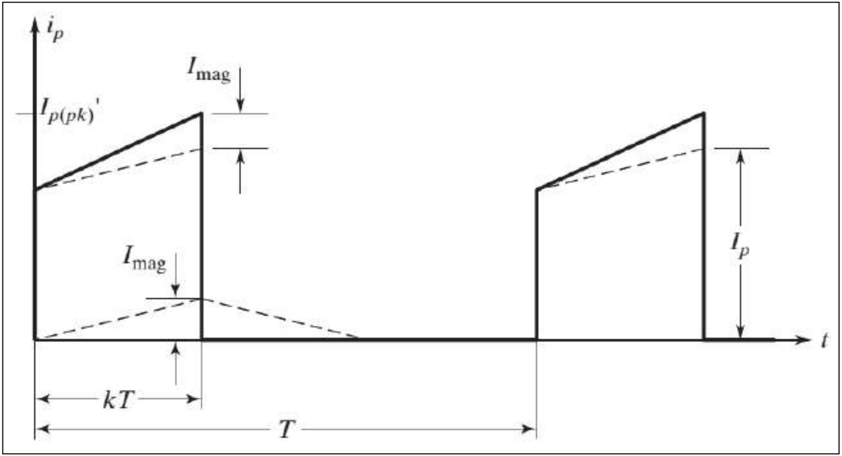


Figure 4 : Current components in primary winding

Mode 1

- Switch Q_1 is turned ON
- Voltage across the primary winding $= V_s$
- D_2 is forward biased
- i_p starts to build up and transfers energy from the primary winding to the secondary and onto the L_1C filter and the load R_L through the rectifier diode D_2
- Primary current, i_p

$$i_p = \frac{N_s}{N_p} i_{se}$$

- Primary magnetizing current i_{mag} rises linearly

$$I_{\text{mag}} = \frac{V_s}{L_p} t$$

- Total primary current i'_p

$$i'_p = i_p + i_{\text{mag}} = \frac{N_s}{N_p} i_{se} + \frac{V_s}{L_p} t$$

- At the end of mode 1 at t = kT, the total primary current reaches a peak value $I'_{p(pk)}$

$$I'_{p(pk)} = I_{p(pk)} + \frac{V_s kT}{L_p}$$

- $I_{p(pk)}$ is the reflected peak current of the output inductor L_1 from the secondary

$$I_{p(pk)} = \left(\frac{N_p}{N_s}\right) I_{L1(pk)}$$

- Voltage developed across the secondary winding

$$V_{se} = \frac{N_s}{N_p} V_s$$

- Voltage across the output inductor L_1 is $(V_{se} - V_o) \rightarrow i_{L1}$ increases linearly

$$\frac{di_{L1}}{dt} = \frac{V_s - V_o}{L_1}$$

- Peak output inductor current $I_{L1(pk)}$ at t = kT,

$$I_{L1(pk)} = I_{L1}(0) + \frac{(V_s - V_o)kT}{L_1}$$

Mode 2

- Q_1 is turned OFF
- Polarity of the transformer voltage reverses
- D_2 turns OFF
- D_1 and D_3 turn ON
- Energy is delivered to R_L through the inductor L_1
- D_1 and tertiary winding provide a path for the magnetizing current returning to the input
- i_{L1} $(= i_{D3})$ decreases linearly

$$i_{L1} = i_{D3} = I_{L1(pk)} - \frac{V_o}{L_1}t \qquad \text{for } 0 < t \leq (1-k)T$$

- In continuous conduction mode operation,

$$I_{L1}(0) = i_{L1}(t = (1-k)T) = I_{L1(pk)} - V_0(1-k)T/L_1$$

Forward Converter

- Output voltage (V_o) = Time integral of secondary winding voltage

$$V_o = \frac{1}{T}\int_0^{kT} \frac{N_s}{N_p} V_s dt = \frac{N_s}{N_p} V_s k$$

- During turn-ON, maximum collector current $I_{C(max)} = I'_{p(pk)}$

$$I_{C(\max)} = I'_{p(pk)} = \left(\frac{N_p}{N_s}\right) I_{L1(pk)} + \frac{V_s kT}{L_p}$$

- During turn-OFF, maximum collector voltage, $V_{Q1(max)}$ = Maximum input voltage, $V_{i(max)}$ + Maximum voltage across the tertiary, $V_{r(max)}$

$$V_{Q1(\max)} = V_{s(\max)} + V_{r(\max)} = V_{s(\max)}\left(1 + \frac{N_p}{N_r}\right)$$

- Time integral of input voltage when Q_1 is ON to the clamping voltage V_r when Q_1 is OFF

$$V_s kT = V_r(1 - k)T$$

- Maximum duty cycle, k_{max}

$$k_{\max} = \frac{1}{1 + N_r/N_p}$$

- k_{max} depends on the turns ratio between the resetting winding and the primary one
- Duty cycle (k) must be less than the maximum duty cycle (k_{max}) to avoid saturating the transformer
- Transformer magnetizing current must be reset to zero at the end of each cycle. Otherwise, the transformer can be driven into saturation, which can cause damage to the switching device
- Tertiary winding is added to the transformer so that the magnetizing current can return to the input source V_s when the transistor turns OFF
- Forward converter is widely used with output power below 200 W

Forward Converter

- A large **load resistance is permanently connected** across the output terminals of forward converter
  - Forward converter requires a minimum load at the output. Otherwise, excess output voltage can be produced
- Since forward converter does not store energy in the transformer, for the same output power level, the **size of the transformer can be made smaller** than that for the flyback.
- **Output current is reasonably constant** due to the action of the output inductor and the freewheeling diode $D_3 \rightarrow$ Output filter capacitor can be made smaller and it's ripple current rating can be much lower than that required for the flyback

Q) The average DC output voltage of the forward converter circuit is $V_o = 24$ V at a resistive load of R = 0.8 Ω. The ON-state voltage drops of transistors and diodes are $V_t = 1.2$ V and $V_d = 0.7$ V respectively. The duty cycle is k = 40% and the switching frequency is f = 1 kHz. The DC supply voltage $V_s = 12$ V. The turns ratio of the transformer is $a = N_s/N_p = 0.25$. Determine

(a) Average input current I_s

(b) Efficiency η

(c) Average transistor current I_A

(d) Peak transistor current I_p

(e) RMS transistor current I_R

(f) Open-circuit transistor voltage V_{oc}

(g) Primary magnetizing inductor L_p for maintaining the peak-to-peak ripple current to 5% of the average input DC current

(h) Output inductor L_1 for maintaining the peak-to-peak ripple current to 4% of its average value. Neglect the losses in the transformer and the ripple content of the output voltage is 3%.

$a = N_s/N_p = 0.25$ and $I_o = V_o/R = 24/0.8 = 30$ A.

a. The output power $P_o = V_o I_o = 24 \times 30 = 720$ W. The secondary voltage $V_2 = V_o + V_d = 24 + 0.7 = 24.7$ V. The primary voltage is $V_1 = V_s - V_t = 12 - 1.2 = 10.8$ V. The turns ratio is $a = V_2/V_1 = 24.7/10.8 = 2.287$. The input power is $P_i = V_s I_s = V_t k I_s + V_d(1-k)I_s + V_d I_o + P_o$ which gives

$$I_s = \frac{V_d I_o + P_o}{V_s - V_t k - V_d(1-k)} = \frac{0.7 \times 30 + 720}{12 - 1.2 \times 0.4 - 0.7 \times 0.6} = 66.76 \text{ A}$$

b. $P_i = V_s I_s = 12 \times 66.756 = 801$ W. The efficiency $\eta = 720/801 = 89.9\%$.

c. $I_A = kI_s = 0.4 \times 66.76 = 26.7$ A.

d. $\Delta I_p = 0.05 \times I_s = 0.05 \times 66.76 = 3.353$ A.

e. $I_R = \sqrt{k}[I_p^2 + {}^{\Delta I_p}/_3 + \Delta I_p I_p]^{1/2} = \sqrt{0.4} \times [66.76^2 + 3.35/3 + 3.35 \times 66.76]^{1/2} = 44.3$ A.

f. $V_{oc} = V_s + V_2/a = 22.8$ V.

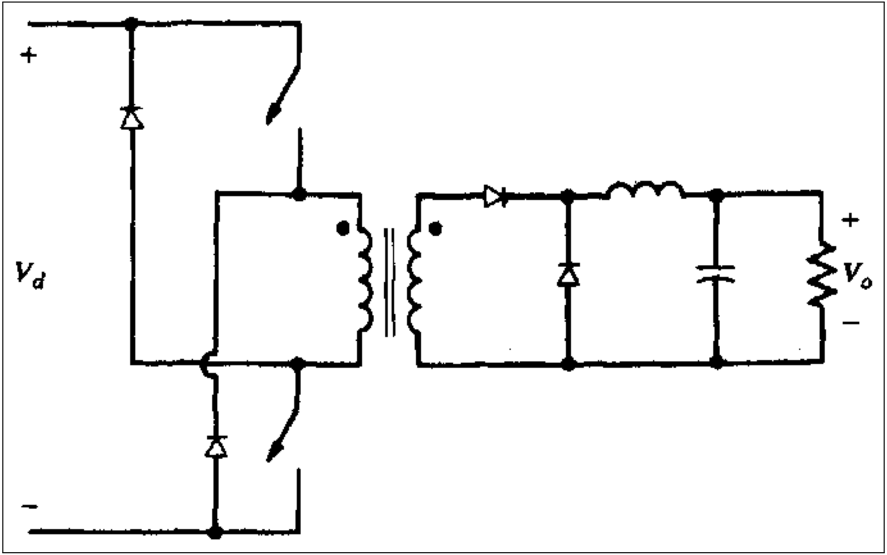
g. $\Delta I_{L1} = 0.04 \times I_o = 0.04 \times 30 = 1.2$ A and $\Delta V_o = 0.03 \times V_o = 0.03 \times 24 = 0.72$ V.

Using Eq. (13.18), $L_1 = \dfrac{\Delta V_o k}{f \Delta I_{L1}} = \dfrac{0.72 \times 0.4}{1 \times 10^3 \times 1.2} = 0.24$ mH

h. Using (13.15), $\Delta I_p = a \times \Delta I_{L1} + (V_s - V_t)kT/L_p$, which gives

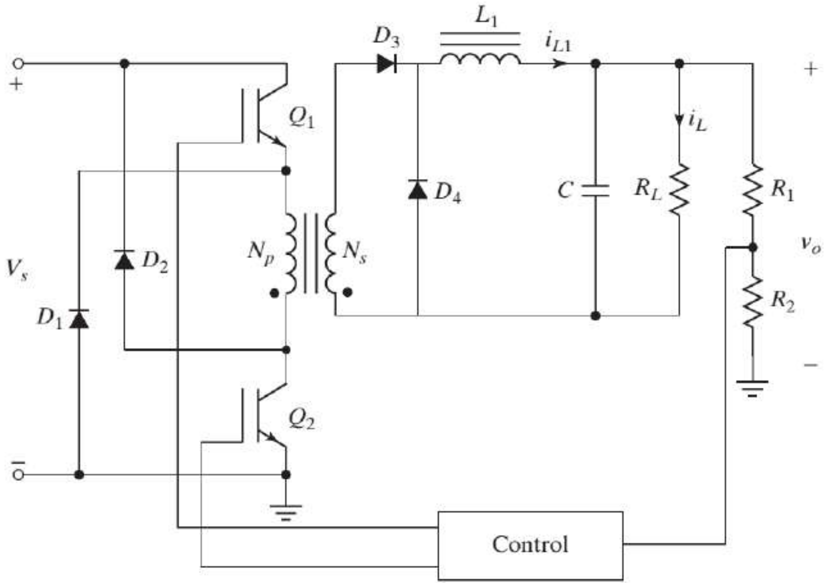
$$L_p = \frac{(V_s - V_t)k}{f(\Delta I_p - a \times \Delta I_{L1})} = \frac{(12 - 1.2) \times 0.4}{1 \times 10^3 \times (3.353 - 2.287 \times 1.2)} = 7.28 \text{ mH}$$

4. Double Ended Forward Converter

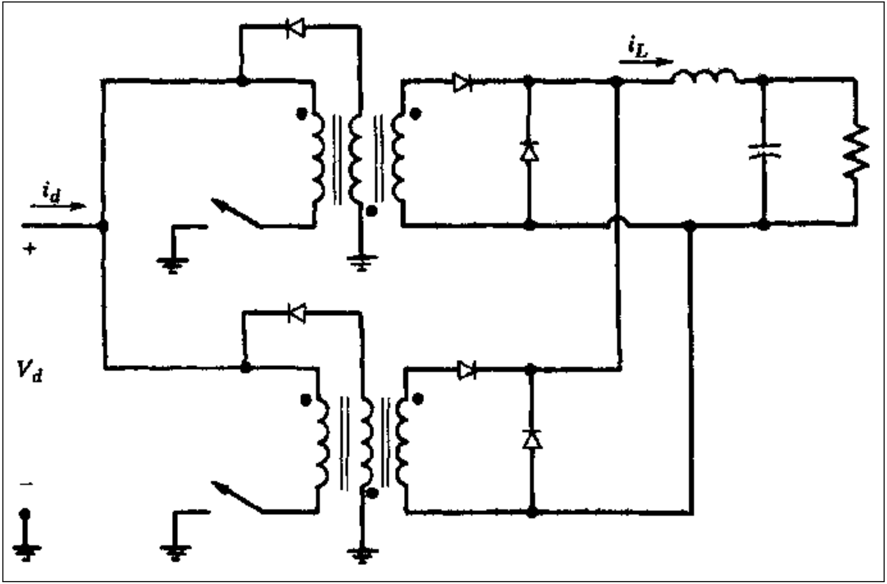


- **Two-Switch Forward Converter**
- Two switches are turned ON and OFF simultaneously
- Voltage rating of each of the switches is one-half of that in a single-switch topology
- Diodes are used to restrict the maximum collector voltage to $V_d \rightarrow$ Switches with low-voltage rating can be used
- When the switches are off, the magnetizing current flows into the input supply through the diodes, thus **eliminating the need for a separate demagnetizing winding or snubbers**

4. Double Ended Forward Converter

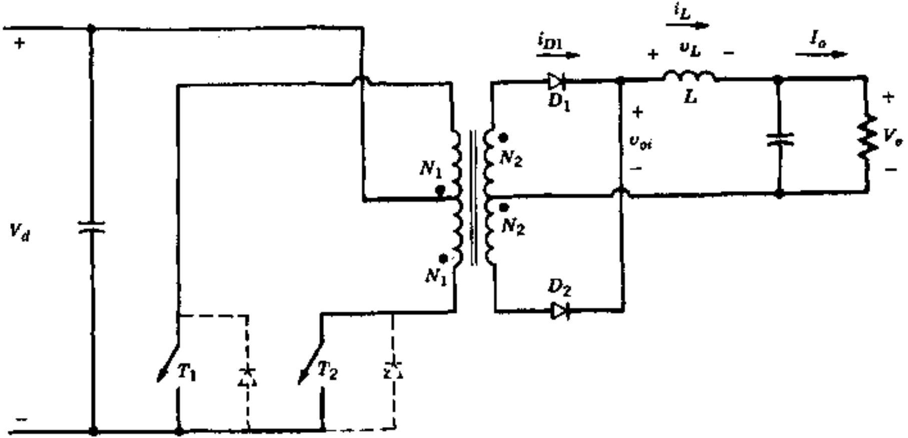


Paralleling Forward Converters

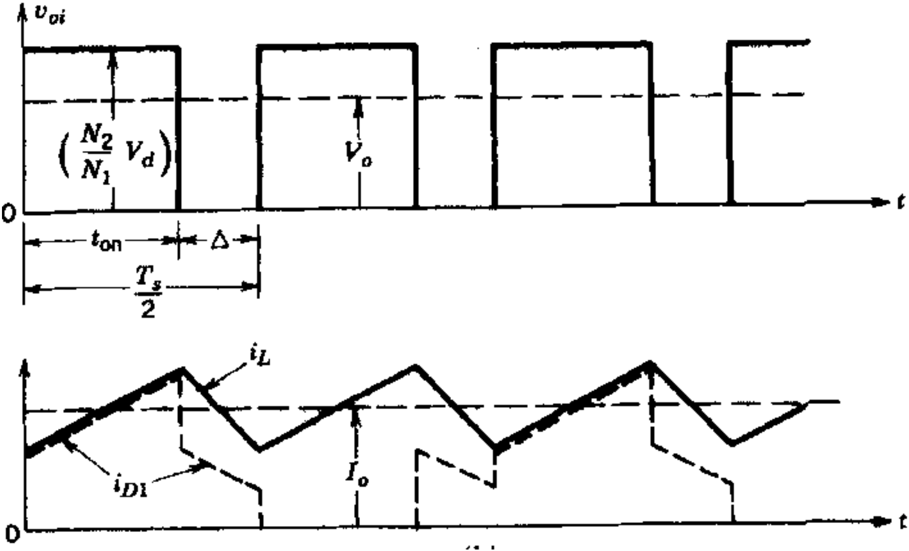


Paralleling Forward Converters

- Switches are sequenced to turn ON a half-time period apart from one another
- At the output, a common filter can be used $\rightarrow$ Significantly reduces the size of the output filter capacitor and inductor



i_L
i_{D1}
I_o
+ v_L −
D_1
L
+
v_{oi}
−
+
V_o
−
+
V_d
−
N_1
N_2
N_2
N_1
D_2
T_1
T_2


v_{oi}
$\left(\frac{N_2}{N_1} V_d\right)$
V_o
0
t
t_{on}
Δ
$\frac{T_s}{2}$
i_L
i_{D1}
I_o
0
t

- Push-Pull inverter is used to produce a square-wave ac at the input of the high-frequency transformer
- Center-tapped secondary of transformer results in only one diode voltage drop on the secondary side

Working

- When T_1 is ON
  - D_1 conducts
  - D_2 gets reverse biased
  - i_L through D_1 increases linearly

$$v_L = \frac{N_2}{N_1}V_d - V_o \qquad 0 < t < t_{on}$$

- When both switches are OFF
  - Interval Δ
  - i_L splits equally between two secondary half-windings
  - $v_{oi} = 0$

$$v_L = -V_o$$

$$i_{D1} = i_{D2} = \frac{1}{2} i_L$$

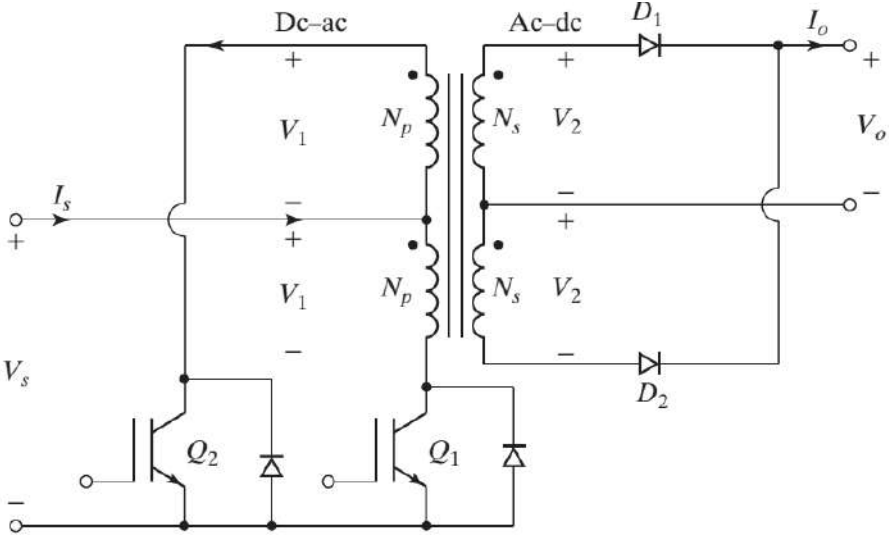
- When T_2 is ON
  - Waveform repeat with a period of $\frac{1}{2} T_s$

$$t_{on} + \Delta = \frac{1}{2} T_s$$

  - Time integral of inductor voltage during one repetition period (ie, $\frac{1}{2} T_s$) is zero

$$\frac{V_o}{V_d} = 2 \frac{N_2}{N_1} D \qquad 0 < D < 0.5$$

  - D $= t_{on}/T_s$, duty ratio of switches T_1 and T_2
- To avoid both switches ON simultaneously, D is kept smaller than 0.5


Dc–ac
Ac–dc
D_1
I_o
$+$
V_1
N_p
N_s
V_2
V_o
I_s
$-$
$+$
V_1
N_p
N_s
V_2
$-$
D_2
V_s
Q_2
Q_1

5. Push-Pull Converter

- When Q_1 is turned on, V_s appears across one-half of the primary
- When Q_2 is turned on, V_s is applied across the other half of the transformer
- Voltage of primary winding swings from $-V_s$ to $+V_s$
- Average current through the transformer should ideally be zero
- Average output voltage,

$$V_o = V_2 = \frac{N_s}{N_p} V_1 = aV_1 = aV_s$$

- Q_1 and Q_2 operate with D$=$ 50%
- $V_{oc} = 2V_s$
- Average current of a transistor, I_A $I_s/2$
- Peak transistor current, $I_p = I_s$
- Since open-circuit transistor voltage is twice the supply voltage, push-pull configuration is suitable for low-voltage applications

Q) The average (DC) output voltage of the pushpull circuit is $V_o = 24$ V at a resistive load of R = 0.8 Ω. The on-state voltage drops of transistors and diodes are $V_t = 1.2$ V and $V_d = 0.7$ V respectively. The turns ratio of the transformer is a $= N_s/N_p = 0.25$. Determine

(a) Average input current, I_s

(b) Efficiency, η

(c) Average transistor current I_A

(d) Peak transistor current, I_p

(e) RMS transistor current, I_R

(f) Open-circuit transistor voltage V_{oc}

Neglect the losses in the transformer and the ripple current of the load and input supply is negligible. Assume duty cycle k = 0.5

Problem

$a = N_s/N_p = 0.25$ and $I_o = V_o/R = 24/0.8 = 30$ A.

a. The output power $P_o = V_o I_o = 24 \times 30 = 720$ W. The secondary voltage $V_2 = V_o + V_d = 24 + 0.7 = 24.7$ V. The primary voltage $V_1 = V_2/a = 24.7/0.25 = 98.8$ V. The input voltage $V_s = V_1 + V_t = 98.8 + 1.2 = 100$ and the input power is

$$P_i = V_s I_s = 1.2 I_A + 1.2 I_A + V_d I_o + P_o$$

Substituting $I_A = I_s/2$ gives

$$I_s(100 - 1.2) = 0.7 \times 30 + 720$$

$$I_s = \frac{741}{98.8} = 7.5 \text{ A}$$

b. $P_i = V_s I_s = 100 \times 7.5 = 750$ W. The efficiency $\eta = 720/750 = 96.0\%$

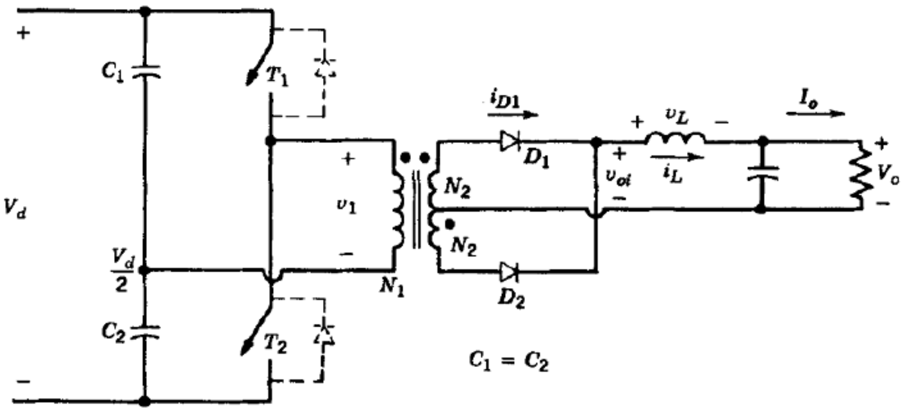
c. $I_A = I_s/2 = 7.5/2 = 3.75$ A.

d. $I_p = I_s = 7.5$ A.

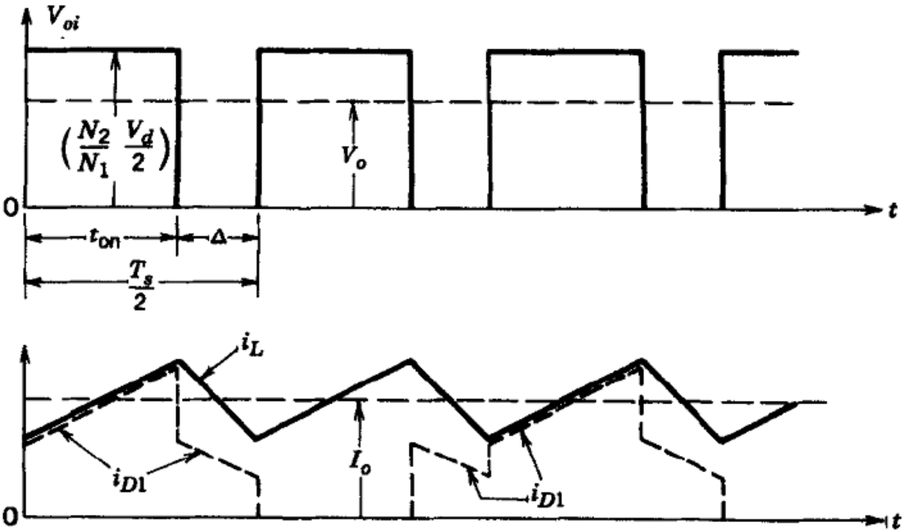
e. $I_R = \sqrt{k} I_p = \sqrt{0.5} \times 7.5 = 5.30$ A, for 50% duty cycle.

f. $V_{oc} = 2V_s = 2 \times 100 = 200\ V$.

6. Half Bridge Converter



6. Half Bridge Converter



- Derived from Buck Converter
- C_1 and C_2 establish a voltage midpoint zero and input DC voltage
- Switches T_1 and T_2 are turned ON alternatively, each for an interval of t_{on}
- When T_1 is ON

$$v_{oi} = (N_2/N_1)(V_d/2)$$

$$v_L = \frac{N_2}{N_1}\frac{V_d}{2} - V_o \qquad 0 < t < t_{on}$$

- When both switches are OFF
  - Interval Δ
  - i_L splits equally between the two secondary halves
  - $v_{oi} = 0$

$$v_L = -V_o \qquad t_{on} < t < t_{on} + \Delta$$

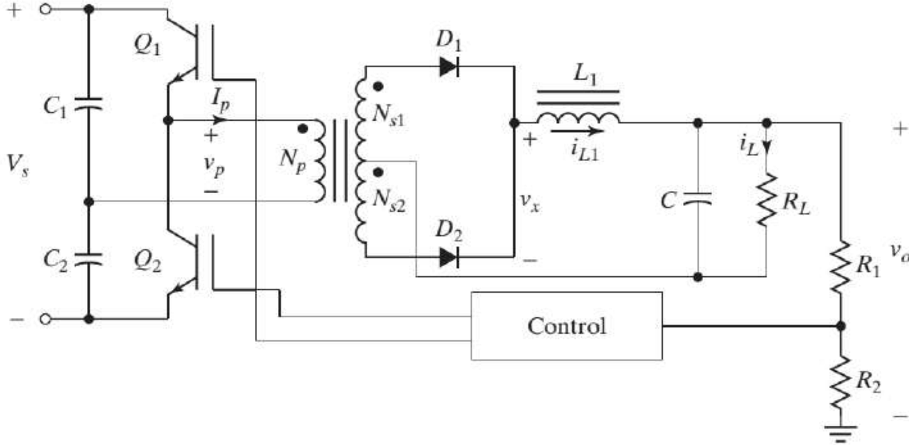
- In steady state, waveforms repeat with a period $\frac{1}{2}T_s$

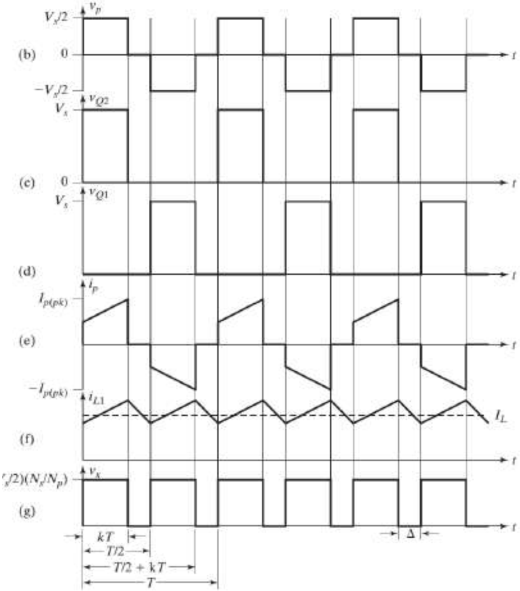
$$t_{on} + \Delta = \frac{1}{2}T_s$$

- Time integral of inductor voltage during one repetition period (ie, $\frac{1}{2}T_s$) is zero

$$\frac{V_o}{V_d} = \frac{N_2}{N_1}D$$

- D $= t_{on}/T_s$
- $0 < D < 0.5$
- Average $v_{oi} = V_o$
- Diodes in antiparallel with Switches T_1 and T_2 are used for switch protection


+
−
V_s
C_1
C_2
Q_1
Q_2
I_p
+
v_p
−
N_p
N_{s1}
N_{s2}
D_1
D_2
L_1
i_{L1}
+
v_x
−
C
i_L
R_L
R_1
R_2
+
v_o
−
Control


v_p
$V_s/2$
(b)
0
$-V_s/2$
v_{Q2}
V_s
(c)
0
v_{Q1}
V_s
(d)
i_p
$I_{p(pk)}$
(e)
$-I_{p(pk)}$
i_{L1}
I_L
(f)
v_x
$(V_s/2)(N_s/N_p)$
(g)
kT
$T/2$
$T/2 + kT$
T
Δ
t

6. Half Bridge Converter

- Half-bridge converter : Two back-to-back forward converters that are fed by the same input voltage, each delivering power to the load at each alternate half-cycle
- C_1 and C_2 are placed across the input terminals such that the voltage across the primary winding always is half of the input voltage ie, $V_s/2$
- Operation
    - Mode 1 : $Q_1 = \text{ON}$ & $Q_2 = \text{OFF}$
    - Mode 2 : Both Q_1 & Q_2 are OFF
    - Mode 3 : $Q_1 = \text{OFF}$ & $Q_2 = \text{ON}$
    - Mode 4 : Both Q_1 & Q_2 are OFF

Mode 1

- $Q_1 = \text{ON}$ and $Q_2 = \text{OFF}$
- D_1 conducts and D_2 is reverse biased
- $V_p = V_s/2$
- i_p starts to build up and stores energy in the primary winding
- Voltage across the secondary winding,

$$V_{se} = \frac{N_{s1}}{N_p}\left(\frac{V_s}{2}\right)$$

- Voltage across the output inductor,

$$v_{L1} = \frac{N_{s1}}{N_p}\left(\frac{V_s}{2}\right) - V_o$$

- Inductor current i_{L1} increases linearly

$$\frac{di_{L1}}{dt} = \frac{v_{L1}}{L_1} = \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_s}{2}\right) - V_o\right]$$

- Peak inductor current $I_{L1(pk)}$ at the end of mode 1 at t = kT

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_s}{2}\right) - V_o\right]kT$$

Mode 2

- For kT $\leq$ t $\leq$ T/2
- Both Q_1 and Q_2 are OFF
- D_1 and D_2 are forced to conduct the magnetizing current that resulted during mode 1
- Rate of fall of i_{L1},

$$\frac{di_{L1}}{dt} = -\frac{V_o}{L_1} \qquad \text{for } 0 < t \leq (0.5 - k)T$$

- $I_{L1}(0) = i_{L1}[t = (0.5 - k)T] = I_{L1(pk)} - V_o(0.5 - k)T/L_1$

Mode 3 and 4

- During mode 3, Q_2 is ON and Q_1 is OFF, D_1 is reverse biased, and D_2 conducts
- $V_p = -V_s/2$
- Mode 4 is similar to mode 2
- Output voltage V_o,

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{kT}\left(\frac{N_{s1}}{N_p}\left(\frac{V_s}{2}\right) - V_o\right)dt + \int_{T/2}^{T/2+kT} -V_o dt\right]$$

$$V_o = \frac{N_{s1}}{N_p} V_s k$$

- Output power P_o,

$$P_o = V_o I_L = \eta P_i = \eta \frac{V_s I_{p(\text{avg})} k}{2}$$

Mode 3 and 4

- Average primary current,

$$I_{p(\text{avg})} = \frac{2P_o}{\eta V_s k}$$

- Assuming that the secondary load current reflected to the primary side is much greater than the magnetizing current, the maximum collector currents for Q_1 and Q_2 are given by

$$I_{C(\max)} = I_{p(\text{avg})} = \frac{2P_o}{\eta V_s k_{\max}}$$

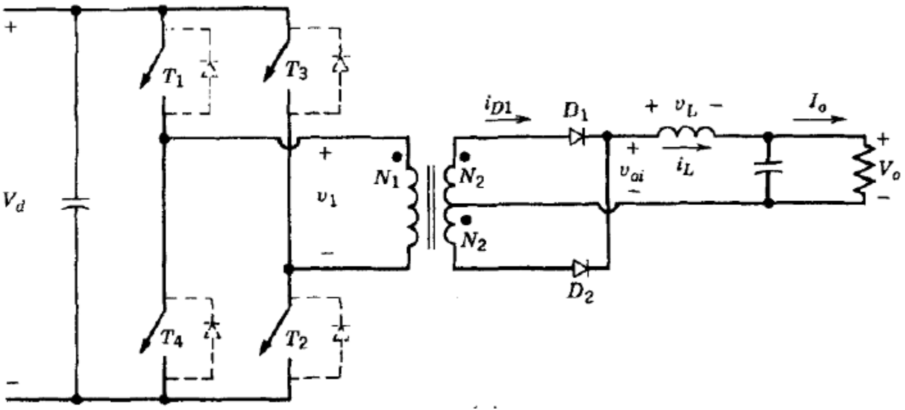
- Maximum collector voltages for Q_1 and Q_2 during turn-off are given by

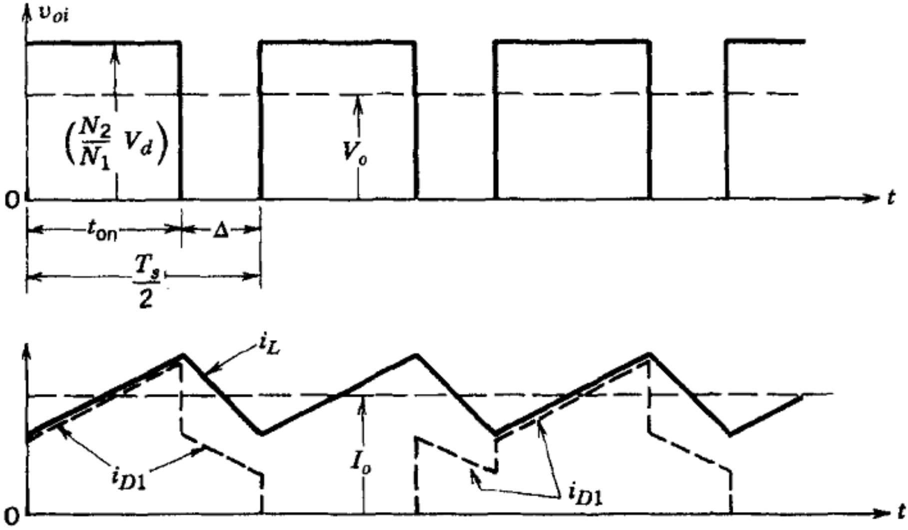
$$V_{C(\max)} = V_{s(\max)}$$

- Maximum duty cycle k can never be greater than 50%
- Half-bridge converter is widely used for medium-power applications (output power ranging from 200 to 400 W)

Forward versus Half-bridge Converter

- In half-bridge converter, the voltage stress imposed on the power transistor is subject to only the input voltage and is only half of that in a forward converter
- Output power of a half-bridge is double to that of a forward converter for the same semiconductor devices and magnetic core
- Since half-bridge is more complex, flyback or forward converter is a better choice and more cost-effective
- Half-bridge converter is unsuitable for high-power applications


+
−
V_d
T_1
T_3
T_4
T_2
+
v_1
−
N_1
N_2
N_2
i_{D1}
D_1
D_2
+ v_L −
i_L
+
v_{oi}
−
I_o
+
V_o
−



v_{oi}
$\left(\frac{N_2}{N_1} V_d\right)$
V_o
0
t
t_{on}
Δ
$\frac{T_s}{2}$
i_L
i_{D1}
I_o
i_{D1}
0
t

- (T_1, T_2) and (T_3, T_4) are switched as pairs alternatively
- When (T_1, T_2) or (T_3, T_4) are ON

$$v_{oi} = (N_2/N_1)V_d$$

$$v_L = \frac{N_2}{N_1}V_d - V_o \qquad 0 < t < t_{\text{on}}$$

- When both (T_1, T_2) and (T_3, T_4) are OFF

$$v_L = -V_o \qquad t_{\text{on}} < t < t_{\text{on}} + \Delta$$

- In steady state, time integral of the inductor voltage over one time period is zero

$$\frac{V_o}{V_d} = 2\frac{N_2}{N_1}D$$

7. Full Bridge Converter

- $t_{on} + \Delta = \frac{1}{2} T_s$
- $\mathrm{D} = \frac{t_{on}}{T_s}$
- $0 < D < 0.5$
- Diodes are connected in antiparallel to the switches to provide a path to the current due to the energy associated with the primary-winding leakage inductance

- Comparison of the full-bridge (FB) converter with half-bridge (HB) converter for **identical input and output voltages and power ratings** requires

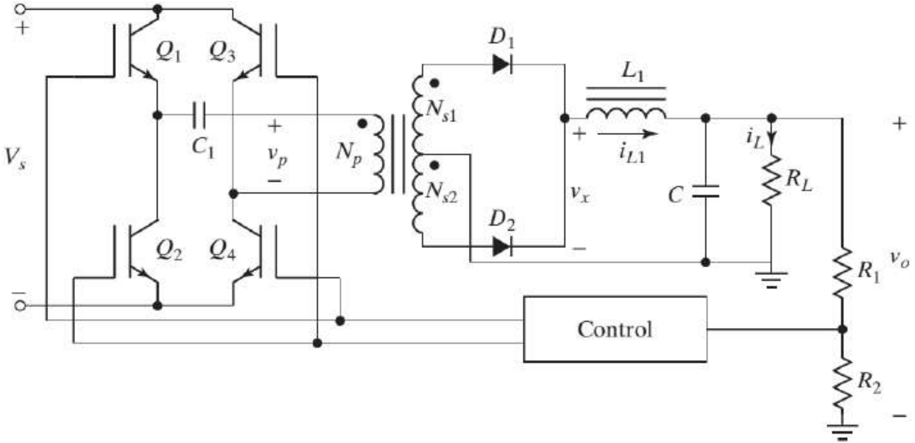
$$\left(\frac{N_2}{N_1}\right)_{HB} = 2\left(\frac{N_2}{N_1}\right)_{FB}$$

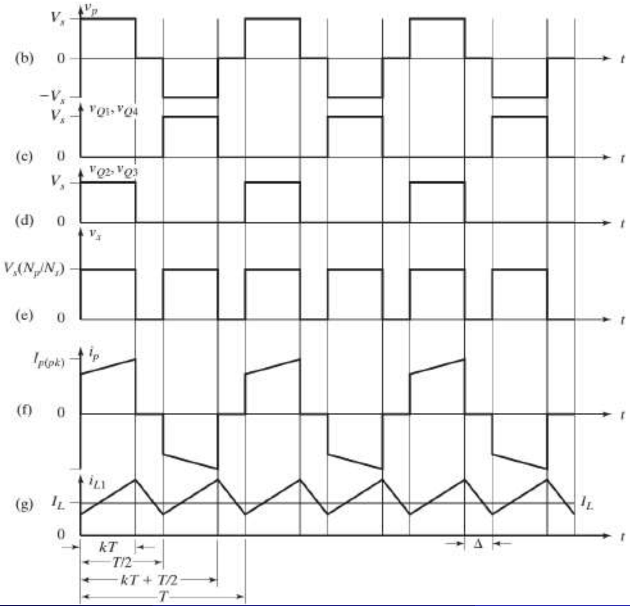
- Neglecting the ripple in the current through the filter inductor at the output and assuming the transformer magnetizing current to be negligible in both circuits, the switch currents are given by

$$(I_{\mathrm{sw}})_{HB} = 2(I_{\mathrm{sw}})_{FB}$$

- In both converters, the input V_d, appears across the switches
- The switches are required to carry twice as much current in the half-bridge compared with the full-bridge converter $\Longrightarrow$ Large power ratings
- It is advantageous to use a full-bridge over a half-bridge converter to

7. Full Bridge Converter





(b)
V_s
v_p
0
$-V_s$
t
(c)
v_{Q1}, v_{Q4}
(d)
v_{Q2}, v_{Q3}
(e)
v_x
$V_s(N_p/N_s)$
(f)
$I_{p(pk)}$
i_p
(g)
i_{L1}
I_L
kT
$T/2$
$kT + T/2$
T
Δ

7. Full Bridge Converter

- Operation
  - Mode 1 : $Q1$ and Q_4 are ON while Q_2 and Q_3 are OFF
  - Mode 2 : All switches are OFF
  - Mode 3 : Q_1 and Q_4 are OFF, while Q_2 and Q_3 are ON
  - Mode 4 : All switches are OFF
- C_1 is used to balance the volt-second integrals during the two half-cycles and prevent the transformer from becoming driven into saturation

Mode 1

- Both Q_1 and Q_4 are turned ON
- Voltage across secondary winding,

$$V_{se} = \frac{N_s}{N_p} V_s$$

- Voltage across the output inductor L_1,

$$v_{L1} = \frac{N_s}{N_p} V_s - V_o$$

- Inductor current i_{L1} increases linearly

$$\frac{di_{L1}}{dt} = \frac{v_{L1}}{L_1} = \frac{1}{L_1}\left[\frac{N_s}{N_p} V_s - V_o\right]$$

- Peak inductor current $I_{L1(pk)}$ at the end of mode 1 at t = kT,

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_s}{N_p} V_s - V_o\right] kT$$

Mode 2

- For kT $\leq$ t $\leq$ T/2
- All switches are OFF
- D_1 and D_2 are forced to conduct the magnetizing current at the end of mode 1
- Rate of fall of i_{L1},

$$\frac{di_{L1}}{dt} = -\frac{V_o}{L_1} \qquad \text{for } 0 < t \leq (0.5 - k)T$$

- $I_{L1(0)} = i_{L1}[t = (0.5 - k)T] = I_{L1(pk)} - V_0(0.5 - k)T/L_1$

Mode 3 and 4

- During mode 3, Q_2 and Q_3 are ON, while Q_1 and Q_4 are OFF
- D_1 is reverse biased and D_2 conducts
- $V_p = V_s$
- Mode 4 is similar to mode 2
- Output voltage V_o,

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{kT}\left(\frac{N_s}{N_p}V_s - V_o\right)dt + \int_{T/2}^{T/2+kT} -V_o\,dt\right]$$

$$V_o = \frac{N_s}{N_p}2V_s k$$

- Output power P_o,

$$P_o = \eta P_i = \eta V_s I_{p(\text{avg})} k$$

Mode 3 and 4

- Average primary current,

$$I_{p(\mathrm{avg})} = \frac{P_o}{\eta V_s k}$$

- Neglecting the magnetizing current, the maximum collector currents for Q_1, Q_2, Q_3 and Q_4 are given by

$$I_{C(\max)} = I_{p(\mathrm{avg})} = \frac{P_o}{\eta V_s k_{\max}}$$

- Maximum collector voltage for Q_1, Q_2, Q_3 and Q_4 during turn-off is given by

$$V_{C(\max)} = V_{s(\max)}$$

Mode 3 and 4

- Full-bridge regulator is used for high-power applications ranging from several hundred to several thousand kilowatts
- It has the most efficient use of magnetic core and semiconductor switches
- Full bridge is complex and therefore expensive to build, and is only justified for high-power applications, typically over 500 W

Half-bridge versus Full-bridge Converter

- Full bridge uses four power switches instead of two, as in the half bridge
- Full bridge converter requires two more gate drivers and secondary windings in the pulse transformer for the gate control circuit
- For the same output power, the maximum collector current of a full bridge is only half that of the half bridge
- Output power of a full bridge is twice that of a half bridge with the same input voltage and current

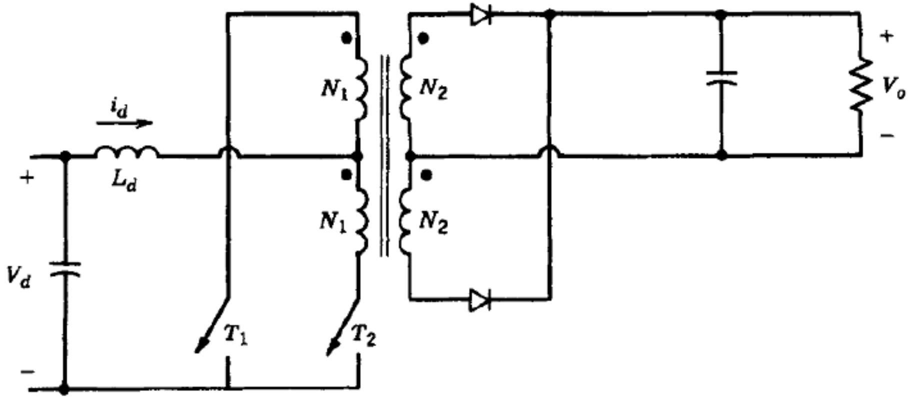


Figure 5 : Current Source Converter (D > 0.5)

- The dc-dc converters with a voltage at their input are referred as voltage source converters
- By inserting an **inductor at the input** of push-pull converter and operating the switches at a duty ratio (D) of greater than 0.5, the converter is fed through a current source
- $D > 0.5 \implies$ Simultaneous conduction of the top switches, which was to be strictly avoided in the normal voltage source push-pull converter

Working

- When both switches are ON, the voltage across each primary half-winding becomes zero
- The input current i_d builds up linearly and the energy is stored in the input inductor
- When only one of the two switches is conducting, the input voltage and the stored energy in the input inductor supply the output stage
- Circuit operates in a manner similar to the step-up converter

Disadvantage

- Current-source converters have a **low power-to-weight ratio** compared to voltage-source converters

References

1. Mohan, Undeland, Robbins, *"Power Electronics Converters Application and Design"*, Wiley-India
2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

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Switched Mode Power Converters

(EE364)

S6-EEE

by

Prof. Dinto Mathew
Asst. Professor
Dept. of EEE, MACE

Module 4 - Overview

1. Switched Mode DC to AC Converter
2. 1-phase Full-bridge Inverter
   - PWM with Bipolar Voltage Switching
   - PWM with Unipolar Voltage Switching
   - Output Control by Voltage Cancellation
   - Switch Utilization in Full Bridge Inverters
3. 3-phase Voltage Source Inverter
   - Sine PWM Inverter
   - Square Wave Operation
   - Switch Utilization in 3-phase Inverter

- Switch-mode DC to AC Inverters

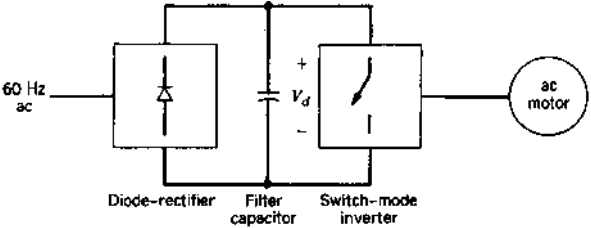


Figure 1 : AC Motor Drive

- Switch-mode DC to AC Inverters

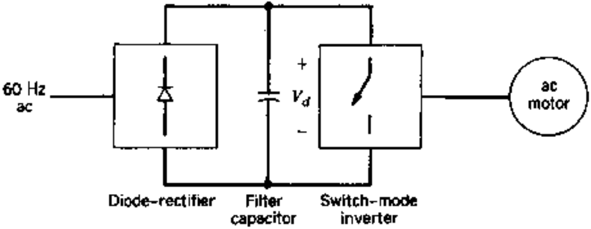


Figure 1 : AC Motor Drive

- To produce sinusoidal AC output whose magnitude and frequency can both be controlled
- **AC motor drives**
  - Diode rectifier → DC voltage is obtained by rectifying and filtering the line voltage
  - Switched Mode DC to AC inverter → AC output
  - Power flow is reversible
- **Uninterruptible AC power supplies**

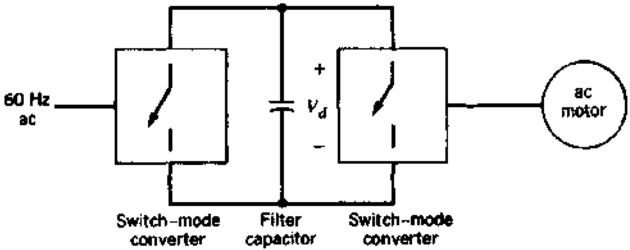
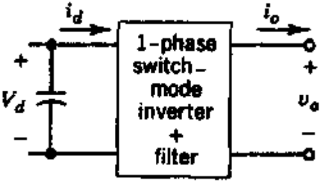


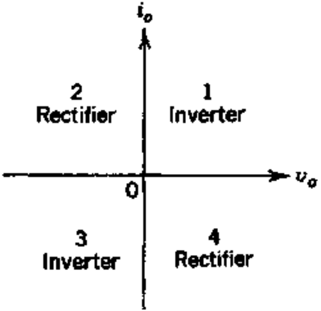
Figure 2 : Switch-mode converters for motoring and regenerative braking in ac motor drive

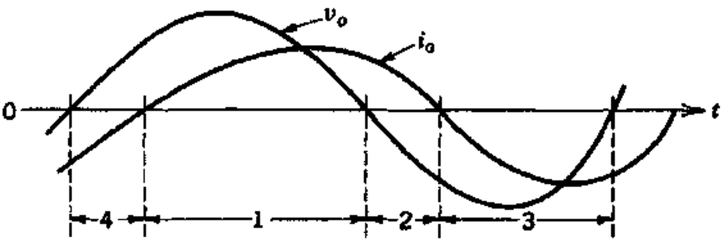
- **Regenerative braking**
  - Energy recovered from the motor load inertia is fed back to the utility grid
  - **Two-quadrant converter** with a reversible dc current, which can operate as a rectifier and as an inverter
  - Two back-to-back connected line-frequency thyristor converters

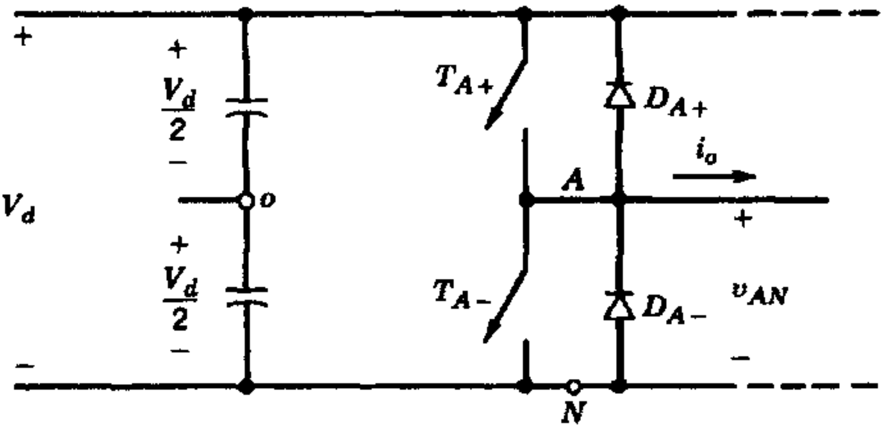
- **Voltage Source Inverters (VSI)** → Input to switch-mode inverters is a DC voltage source
  1. **Pulse-width-modulated Inverters**
     - Input DC voltage is constant in magnitude
     - Inverter must control the magnitude and the frequency of the AC output voltages
     - Pulse-width Modulation of Inverter → Sinusoidal PWM
  2. **Square-wave Inverters**
     - Input DC voltage is controlled in order to control the magnitude of the output AC voltage
     - Hence inverter has to control only the frequency of the output voltage
     - Output AC voltage has a waveform similar to a square wave $\Longrightarrow$ Square wave inverter
  3. **Single-phase inverters with voltage cancellation**
     - These inverters combine the characteristics PWM and Square wave inverters
     - Control the magnitude and the frequency of the inverter output voltage, even though the input to the inverter is a constant DC voltage and the inverter switches are not pulse-width modulated
     - Voltage cancellation technique works only with single-phase inverters and not with three-phase inverter

- **Current Source Inverters (CSI)** $\rightarrow$ DC input to the inverter is a dc current source
    - Very high power AC motor drives


i_d
i_o
1-phase switch-mode inverter + filter
V_d
v_o
+
−
+
−


i_o
2 Rectifier
1 Inverter
0
v_o
3 Inverter
4 Rectifier


v_o
i_o
0
t
4
1
2
3


+
+
$\frac{V_d}{2}$
−
V_d
o
+
$\frac{V_d}{2}$
−
−
T_{A+}
D_{A+}
i_o
A
+
T_{A-}
D_{A-}
v_{AN}
−
N

- Single-phase inverter
- Output voltage of the inverter is filtered $\Longrightarrow$ sinusoidal
- Inverter supplies an inductive load
- Output waveforms
  - Interval 1 : v_o and i_o are both positive
  - Interval 3 : v_o and i_o are both negative
  - During intervals 1 and 3, the instantaneous power flow $p_o ie, (= v_o i_o,)$ is from the DC side to the AC side, corresponding to an inverter mode of operation
  - In intervals 2 and 4 p_o flows from the AC side to the DC side of the inverter, corresponding to a rectifier mode of operation
- Switch-mode inverter is capable of operating in all four quadrants of the $i_o - v_o$

Pulse Width Modulated Switching Scheme

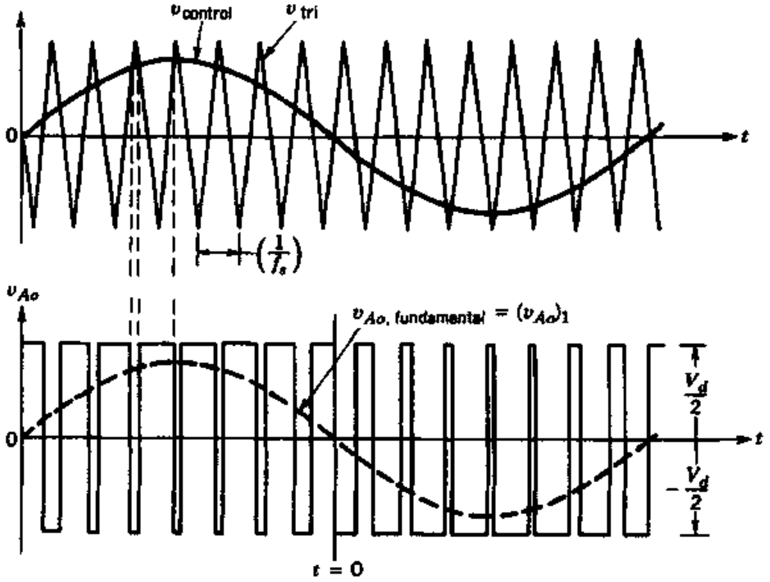
- For an inverter to produce sinusoidal output
  - A sinusoidal control signal at the desired frequency is compared with a triangular waveform
  - Frequency of the triangular waveform establishes the inverter switching frequency (f_s)
  - Frequency and amplitude ($\widehat{V}_{tri}$) of triangular waveform are kept constant
- $v_{control}$ has a frequency f_i, which is the desired fundamental frequency of the inverter voltage output
- **Amplitude Modulation Ratio (m_a)**

$$m_a = \frac{\hat{V}_{\text{control}}}{\hat{V}_{\text{tri}}}$$

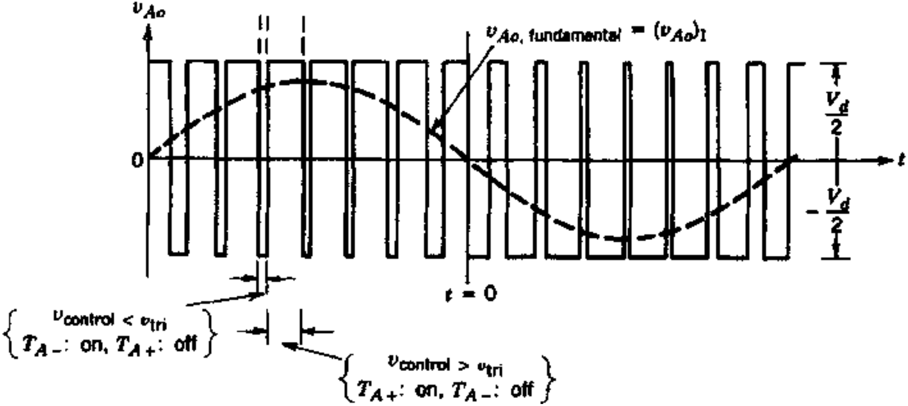
- **Frequency Modulation Ratio (m_f)**

$$m_f = \frac{f_s}{f_1}$$

Pulse Width Modulated Switching Scheme



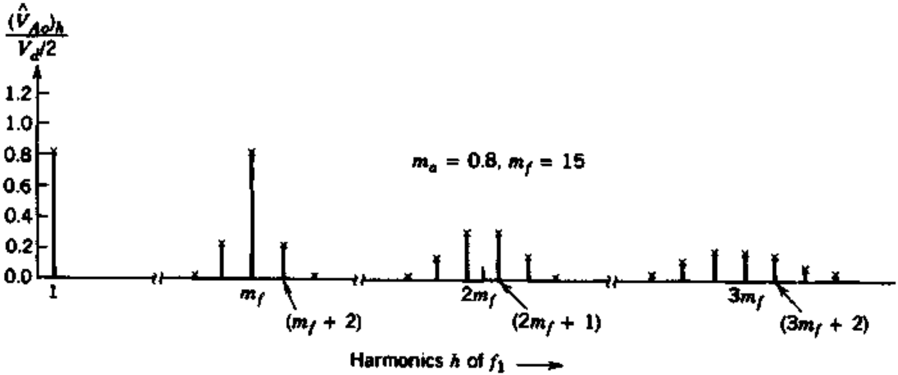
Pulse Width Modulated Switching Scheme



- In the inverter, switches are controlled such that

$$v_{\text{control}} > v_{\text{tri}}, \qquad T_{A+} \text{ is on}, \qquad v_{Ao} = \frac{1}{2}V_d$$

$$v_{\text{control}} < v_{\text{tri}}, \qquad T_{A-} \text{ is on}, \qquad v_{Ao} = -\frac{1}{2}V_d$$



Pulse Width Modulated Switching Scheme

- Output voltage (v_{Ao}) fluctuates between ($\frac{1}{2}V_d$) and ($\frac{-1}{2}V_d$)

Harmonic spectrum of V_{Ao} shows that

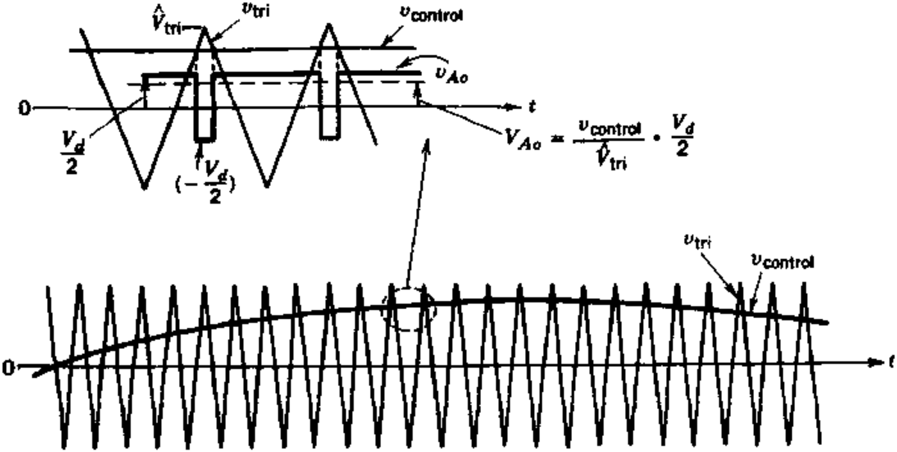
- Peak amplitude of the fundamental-frequency component $(\hat{V}_{Ao})_1$ is m_a times ($\frac{1}{2}V_d$)

$$V_{Ao} = \frac{v_{\text{control}}}{\hat{V}_{\text{tri}}}\frac{V_d}{2} \qquad v_{\text{control}} \leq \hat{V}_{\text{tri}}$$

- Let $v_{control}$ varies sinusoidally at the frequency f $= \omega_1/2\pi$

$$v_{\text{control}} = \hat{V}_{\text{control}} \sin \omega_1 t$$

$$\hat{V}_{\text{control}} \leq \hat{V}_{\text{tri}}$$



$\hat{V}_{tri}$
v_{tri}
$v_{control}$
v_{Ao}
0
t
$\frac{V_d}{2}$
$(-\frac{V_d}{2})$
$V_{Ao} = \frac{v_{control}}{\hat{V}_{tri}} \cdot \frac{V_d}{2}$
v_{tri}
$v_{control}$
0
t

$$(v_{Ao})_1 = \frac{\hat{V}_{\text{control}}}{\hat{V}_{\text{tri}}} \sin \omega_1 t \, \frac{V_d}{2}$$

$$= m_a \sin \omega_1 t \, \frac{V_d}{2} \quad \text{for } m_a \leq 1.0$$

Range of m_a from 0 to 1 is referred to as **linear range**

$$(\hat{V}_{Ao})_1 = m_a \frac{V_d}{2} \qquad m_a \leq 1.0$$

- Harmonics in the inverter output voltage waveform appear as sidebands, centered around the switching frequency and its multiples ie, around harmonics m_f, $2m_f$, $3m_f$, and so on
  - This pattern holds true for all values of m_a in the range 0 - 1
  - Frequency modulation ratio $m_f \leq 9$

$$f_h = (jm_f \pm k)f_1 \qquad h = j(m_f) \pm k$$

$$v_{AN} = v_{Ao} + \tfrac{1}{2}V_d \qquad (\hat{V}_{AN})_h = (\hat{V}_{Ao})_h$$

h \ m_a	0.2	0.4	0.6	0.8	1.0
1 Fundamental	0.2	0.4	0.6	0.8	1.0
m_f	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.008	0.105	0.068
$4m_f \pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.050

Note: $(\hat{V}_{Ao})_h/(\frac{1}{2}V_d)$ [$= (\hat{V}_{AN})_h/(\frac{1}{2}V_d)$] is tabulated as a function of m_a.

Pulse Width Modulated Switching Scheme

- m_f should be an odd integer
  - It results in an odd symmetry [f(-t) = -f(t)] as well as a half-wave symmetry [f(t) = -f(t+1/2T_1)] with the time origin
  - Only odd harmonics are present and the even harmonics disappear from the waveform of V_{Ao}
  - Only the coefficients of the sine series in the Fourier analysis are finite and those for the cosine series are zero

Problem

Q) For a single phase half bridge inverter, $V_d = 300$ V, $m_a = 0.8$, $m_f = 39$ and the fundamental frequency is 47 Hz. Calculate the rms values of the fundamental-frequency voltage and some of the dominant harmonics in V_{Ao}.

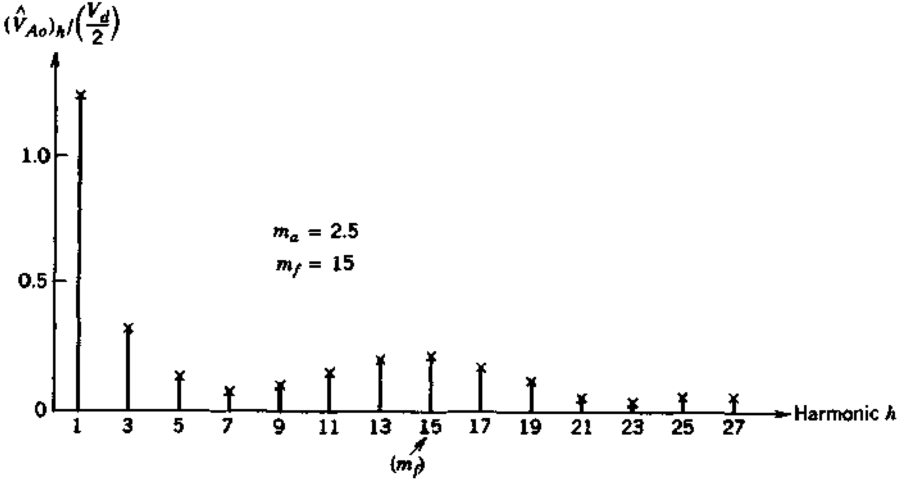
$$(V_{Ao})_h = \frac{1}{\sqrt{2}} \frac{V_d}{2} \frac{(\hat{V}_{Ao})_h}{V_d/2}$$

$$= 106.07 \frac{(\hat{V}_{Ao})_h}{V_d/2}$$

$$\begin{aligned}
(V_{Ao})_1 &= 106.07 \times 0.8 = 84.86\ V \quad \text{at 47 Hz} \\
(V_{Ao})_{37} &= 106.07 \times 0.22 = 23.33\ V \quad \text{at 1739 Hz} \\
(V_{Ao})_{39} &= 106.07 \times 0.818 = 86.76\ V \quad \text{at 1833 Hz} \\
(V_{Ao})_{41} &= 106.07 \times 0.22 = 23.33\ V \quad \text{at 1927 Hz} \\
(V_{Ao})_{77} &= 106.07 \times 0.314 = 33.31\ V \quad \text{at 3619 Hz} \\
(V_{Ao})_{79} &= 106.07 \times 0.314 = 33.31\ V \quad \text{at 3713 Hz}
\end{aligned}$$

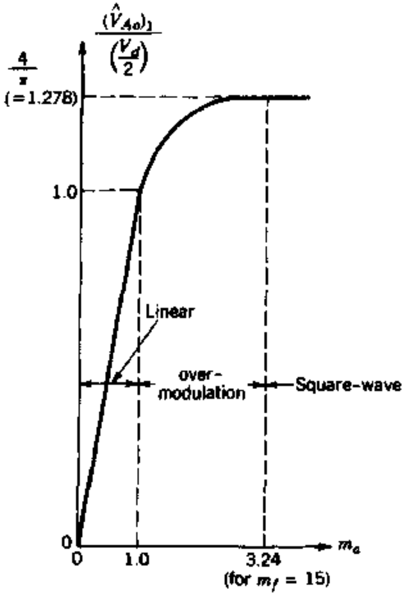
Over-modulation ($m_a < 1$)

- To increase further the amplitude of the fundamental frequency component in the output voltage, m_a is increased beyond 1.0 $\Longrightarrow$ **Over-modulation**
- Over-modulation causes the output voltage to contain many more harmonics in the side-bands as compared with the linear range (with $m_a \leq 1$)
- With over-modulation, the amplitude of the fundamental- frequency component does not vary linearly with the amplitude modulation ratio m_a



$(\hat{V}_{Ao})_h/\left(\frac{V_d}{2}\right)$
1.0
0.5
0
$m_a = 2.5$
$m_f = 15$
1
3
5
7
9
11
13
15
17
19
21
23
25
27
(m_f)
Harmonic h

Pulse Width Modulated Switching Scheme



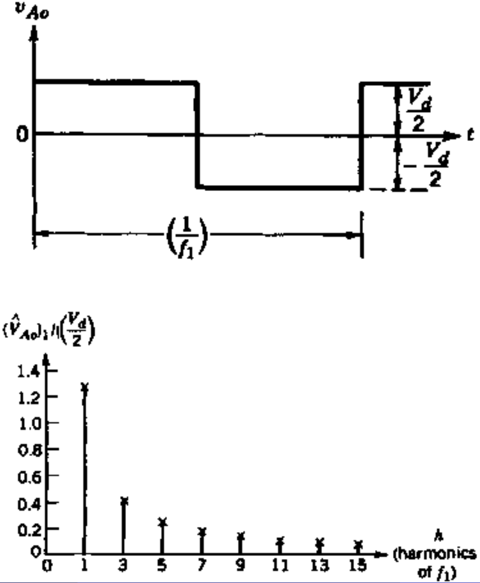
Square Wave Switching Scheme

- Each switch of the inverter leg is ON for one half-cycle (180^o) of the desired output frequency
- Peak value of the fundamental-frequency

$$(\hat{V}_{Ao})_1 = \frac{4}{\pi}\frac{V_d}{2} = 1.273\left(\frac{V_d}{2}\right)$$

$$(\hat{V}_{Ao})_h = \frac{(\hat{V}_{Ao})_1}{h}$$

- Harmonic order h takes on only odd values
- Square-wave switching is a special case of the sinusoidal PWM switching when m_a becomes so large that the control voltage waveform intersects with the triangular waveform only at the zero crossing of $v_{control}$
- Output voltage is independent of m_a in the square-wave region



v_{Ao}
0
$\frac{V_d}{2}$
t
$-\frac{V_d}{2}$
$\left(\frac{1}{f_1}\right)$
$(\hat{V}_{Ao})_h / \left(\frac{V_d}{2}\right)$
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0 1 3 5 7 9 11 13 15
h (harmonics of f_1)

Square Wave Switching Scheme

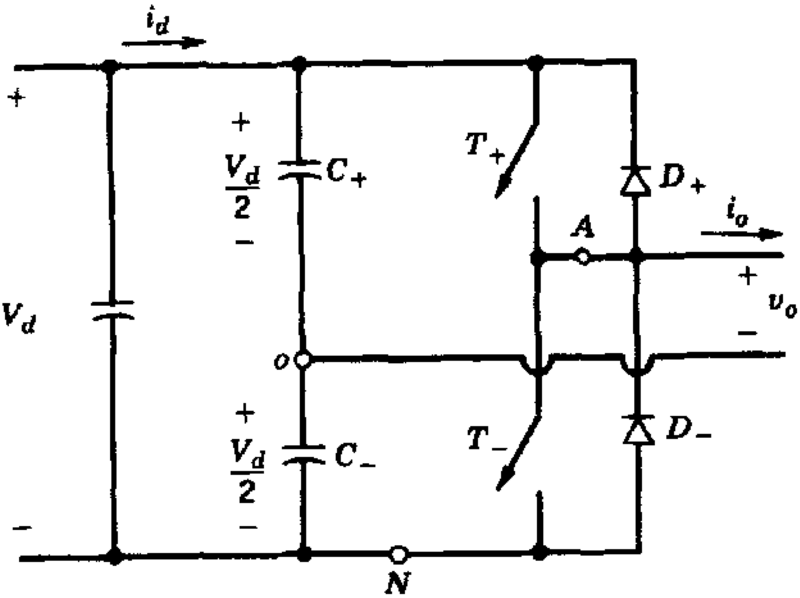
Advantage

- Each inverter switch changes its state only twice per cycle, which is important at very high power levels where the solid-state switches generally have slower turn-on and turn-off speeds

Disadvantage

- Inverter is not capable of regulating the output voltage magnitude. Therefore, the DC input voltage (V_d), to the inverter must be adjusted in order to control the magnitude of the inverter output voltage

1-phase Half-bridge Inverter



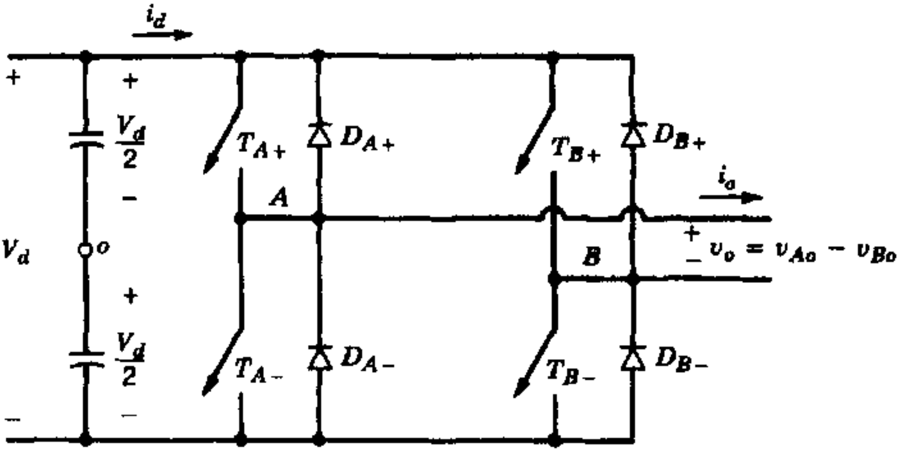
1-phase Half-bridge Inverter

- Circuit configuration is identical to the basic one-leg inverter
- $v_o = V_{Ao}$
- Regardless of the switch states, the current between the two capacitors C_+ and C_- divides equally
- When T_+ is ON, either T_+ or D_+ conducts depending on the direction of i_o
- When the switch T_- is ON, either T_- or D_- conducts depending on the direction of i_o
- In half-bridge inverter, the peak voltage rating of switch

$$V_T = V_d$$

- In half-bridge inverter, the peak current rating of switch

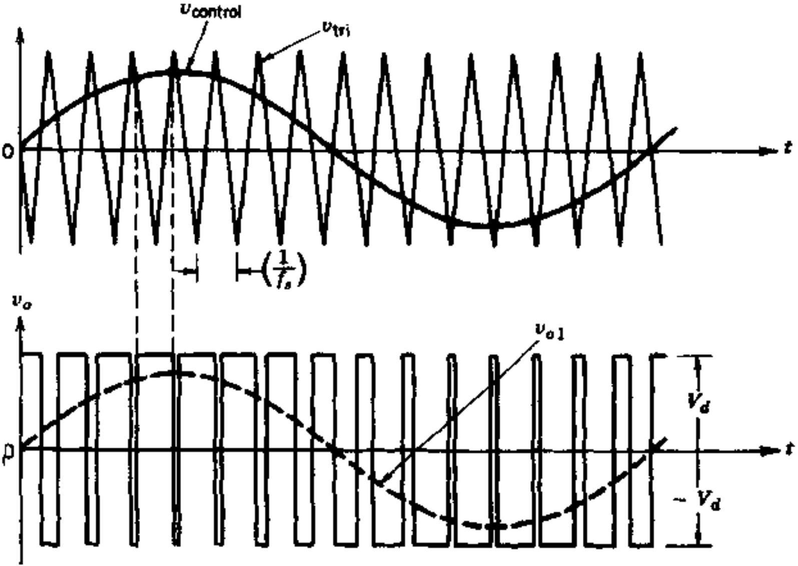
$$I_T = i_{o,\text{peak}}$$


i_d
+
+
$\frac{V_d}{2}$
−
V_d
o
+
$\frac{V_d}{2}$
−
−
T_{A+}
D_{A+}
T_{B+}
D_{B+}
A
B
i_o
+
−
$v_o = v_{Ao} - v_{Bo}$
T_{A-}
D_{A-}
T_{B-}
D_{B-}

2. 1-phase Full-bridge Inverter

- 1-phase Full-bridge inverter consists of two one-leg inverters
- Higher power ratings
- With the same dc input voltage, the maximum output voltage of the full-bridge inverter is twice that of the half-bridge inverter
- Output current and the switch currents of full bridge inverter are one-half of those for a half-bridge inverter

2.1 PWM with Bipolar Voltage Switching



- Switch pairs : (T_{A+}, T_{B-}) and (T_{A-}, T_{B+})
- Output of inverter leg B is negative of the leg A output
- When T_{A+} is ON, $V_{Ao} = \frac{V_d}{2}$
- When T_{B-} is ON, $V_{Bo} = \frac{-V_d}{2}$

$$v_{Bo}(t) = -v_{Ao}(t)$$

$$v_o(t) = v_{Ao}(t) - v_{Bo}(t) = 2v_{Ao}(t)$$

- Peak of the fundamental-frequency component in the output voltage $(\hat{V}_{01})$

$$\hat{V}_{o1} = m_a V_d \qquad (m_a \leq 1.0)$$

$$V_d < \hat{V}_{o1} < \frac{4}{\pi} V_d \qquad (m_a > 1.0)$$

- v_o switches between $-V_d$ and $+V_d$ voltage levels $\implies$ **PWM with Bipolar Voltage Switching**

Problem

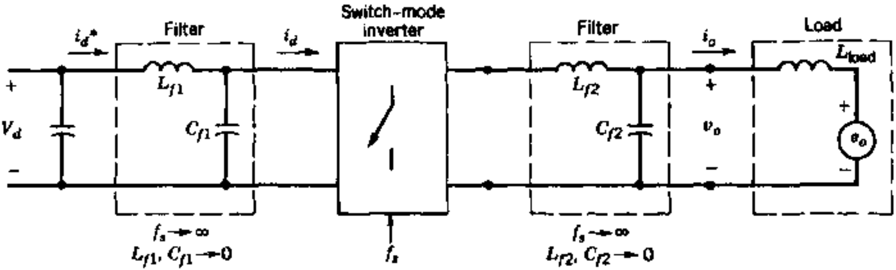
Q) In the full-bridge converter circuit, $V_d = 300$ V, $m_a = 0.8$, $m_f = 39$ and the fundamental frequency is 47 Hz. Calculate the rms values of the fundamental-frequency voltage and some of the dominant harmonics in the output voltage v_o if a PWM bipolar voltage-switching scheme is used.

$$(V_o)_h = \frac{1}{\sqrt{2}} \cdot 2 \cdot \frac{V_d}{2} \frac{(\hat{V}_{Ao})_h}{V_d/2} = \frac{V_d}{\sqrt{2}} \frac{(\hat{V}_{Ao})_h}{V_d/2}$$

$$= 212.13 \frac{(\hat{V}_{Ao})_h}{V_d/2}$$

$$\begin{aligned}
V_{o1} &= 212.13 \times 0.8 = 169.7\ V \quad \text{at 47 Hz} \\
(V_o)_{37} &= 212.13 \times 0.22 = 46.67\ V \quad \text{at 1739 Hz} \\
(V_o)_{39} &= 212.13 \times 0.818 = 173.52\ V \quad \text{at 1833 Hz} \\
(V_o)_{41} &= 212.13 \times 0.22 = 46.67\ V \quad \text{at 1927 Hz} \\
(V_o)_{77} &= 212.13 \times 0.314 = 66.60\ V \quad \text{at 3619 Hz} \\
(V_o)_{79} &= 212.13 \times 0.314 = 66.60\ V \quad \text{at 3713 Hz}
\end{aligned}$$

DC Side Current (i_d)



- Switching frequency is assumed to be very high, approaching infinity $\Longrightarrow$ To filter out the high-switching-frequency components in v_o and i_d, the filter components L and C required in both AC and DC side filters approach zero. ie, the energy stored in the filters is negligible. Since the converter itself has no energy storage elements, the instantaneous power input must equal the instantaneous power output

- Sine wave at the fundamental output frequency ω_1

$$v_{o1} = v_o = \sqrt{2}V_o \sin \omega_1 t$$

- Output current (i_o)

$$i_o = \sqrt{2}I_o \sin(\omega_1 t - \phi)$$

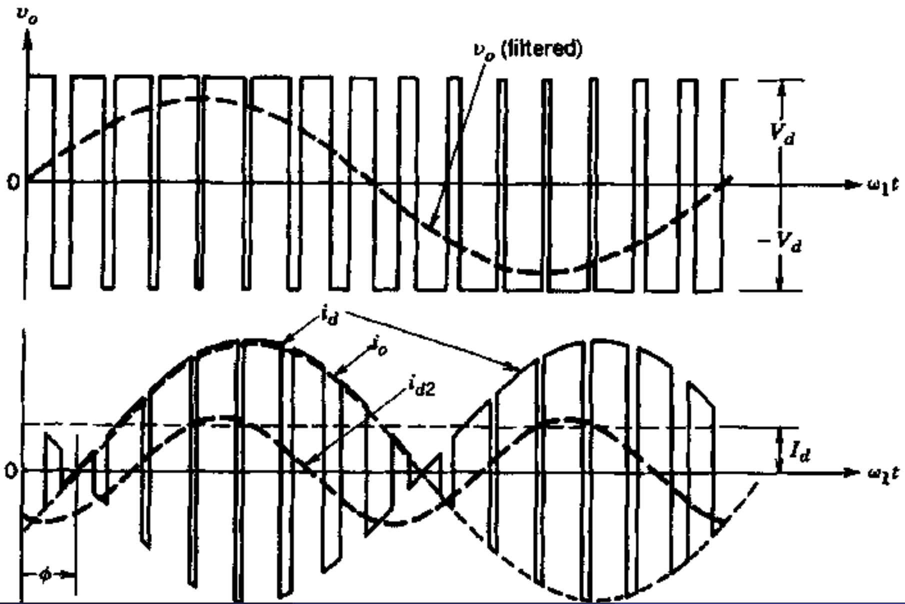
- Assuming that no energy is stored in the filters

$$V_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2}V_o \sin \omega_1 t \sqrt{2}I_o \sin(\omega_1 t - \phi)$$

$$\begin{aligned} i_d^*(t) &= \frac{V_o I_o}{V_d}\cos\phi - \frac{V_o I_o}{V_d}\cos(2\omega_1 t - \phi) = I_d + i_{d2} \\ &= I_d - \sqrt{2}I_{d2}\cos(2\omega_1 t - \phi) \end{aligned}$$

$$I_d = \frac{V_o I_o}{V_d}\cos\phi \qquad I_{d2} = \frac{1}{\sqrt{2}}\frac{V_o I_o}{V_d}$$

- i_d^* consists of
  1. I_d : DC component $\rightarrow$ responsible for the power transfer from V_d on the DC side of the inverter to the AC side
  2. Sinusoidal component at twice the fundamental frequency due to inverter switchings



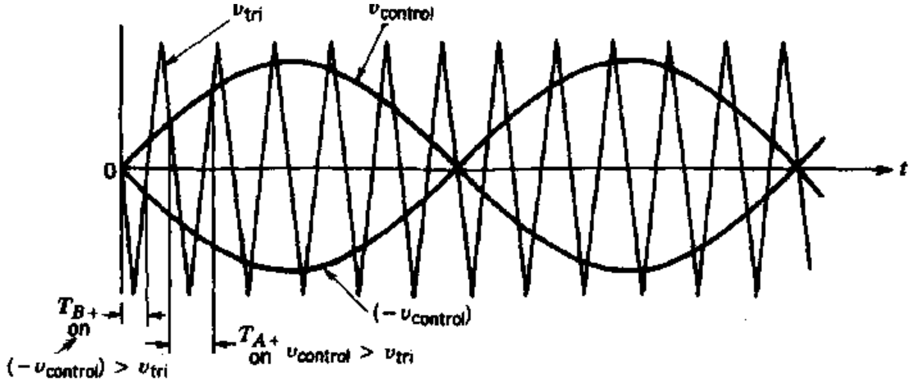
v_o
v_o (filtered)
0
V_d
$-V_d$
$\omega_1 t$
i_d
i_o
i_{d2}
0
I_d
$\omega_1 t$
ϕ

- Unipolar voltage switching
  - Legs A and B of the full-bridge inverter are controlled separately by comparing V_{tri} with $v_{control}$ and $-v_{control}$ respectively
- Leg A

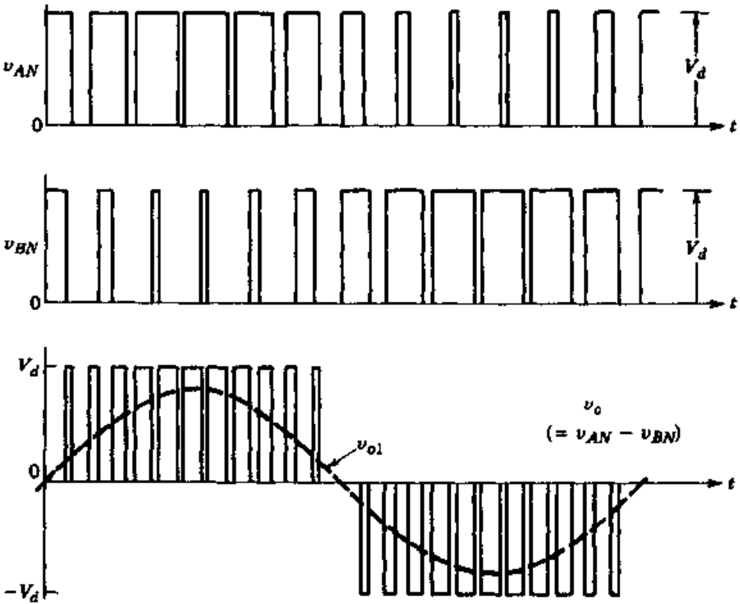
$$
\begin{aligned}
v_{\text{control}} > v_{\text{tri}}: &\quad T_{A+} \text{ on} \quad \text{and} \quad v_{AN} = V_d \\
v_{\text{control}} < v_{\text{tri}}: &\quad T_{A-} \text{ on} \quad \text{and} \quad v_{AN} = 0
\end{aligned}
$$

- Leg B

$$
\begin{aligned}
(-v_{\text{control}}) > v_{\text{tri}}: &\quad T_{B+} \text{ on} \quad \text{and} \quad v_{BN} = V_d \\
(-v_{\text{control}}) < v_{\text{tri}}: &\quad T_{B-} \text{ on} \quad \text{and} \quad v_{BN} = 0
\end{aligned}
$$



v_{tri}
$v_{control}$
0
t
$(-v_{control})$
T_{B+} on
$(-v_{control}) > v_{tri}$
T_{A+} on
$v_{control} > v_{tri}$

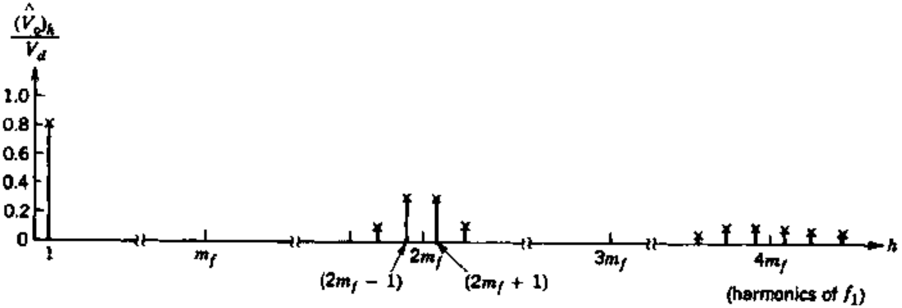


v_{AN}
V_d
0
t
v_{BN}
V_d
0
t
V_d
0
$-V_d$
v_{o1}
v_o
$(= v_{AN} - v_{BN})$
t

1. T_{A+}, T_{B-} on: $v_{AN} = V_d, \quad v_{BN} = 0; \quad v_o = V_d$
2. T_{A-}, T_{B+} on: $v_{AN} = 0, \quad v_{BN} = V_d; \quad v_o = -V_d$
3. T_{A+}, T_{B+} on: $v_{AN} = V_d, \quad v_{BN} = V_d; \quad v_o = 0$
4. T_{A-}, T_{B-} on: $v_{AN} = 0, \quad v_{BN} = 0; \quad v_o = 0$

- When both the upper switches are ON
  - Output voltage is zero
  - i_o circulates in a loop through (T_{A+} and D_{B+}) or (D_{A+} and T_{B+}) depending on the direction of i_o
  - Input current i_d is zero
- In **unipolar PWM scheme**, v_o changes between zero and $+V_d$ or between zero and $-V_d$ voltage levels
- It has the advantage of **effectively doubling the switching frequency** as far as the output harmonics are concerned, compared to the bipolar voltage-switching scheme
- Also the voltage jumps in the output voltage at each switching are reduced to V_d

Harmonic Analysis



Harmonic Analysis

- **Effectively doubling the switching frequency** appears in the harmonic spectrum of the output voltage waveform
- Lowest harmonics appear as side-bands of twice the switching frequency
- Lets consider modulation ratio m_f to be even
- v_{AN} and v_{BN} are displaced by 180^o of the fundamental frequency f, with respect to each other
- Harmonic components at the switching frequency in v_{AN} and v_{BN} have the same phase $\rightarrow$ Cancellation of the harmonic component at the switching frequency in v_o
- Side-bands of the switching-frequency harmonics disappear
- Other dominant harmonic at twice the switching frequency cancels out, while its side-bands do not

$$\hat{V}_{o1} = m_a V_d \qquad (m_a \leq 1.0)$$

$$V_d < \hat{V}_{o1} < \frac{4}{\pi} V_d \qquad (m_a > 1.0)$$

Problem

Q) Consider a PWM with unipolar voltage switching scheme with $m_f = 38$. Calculate the rms values of the fundamental frequency voltage and some of the dominant harmonics in the output voltage. f = 47 Hz

$$h = j(2m_f) \pm k$$

$$(V_o)_h = 212.13 \frac{(V_{Ao})_h}{V_d/2}$$

At fundamental or 47 Hz: $V_{o1} = 0.8 \times 212.13 = 169.7\ V$

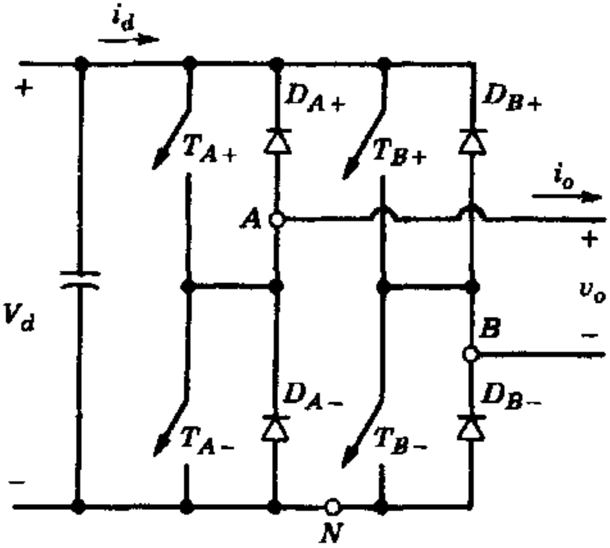
At $h = 2m_f - 1 = 75$ or $3525\ Hz$: $(V_o)_{75} = 0.314 \times 212.13 = 66.60\ V$

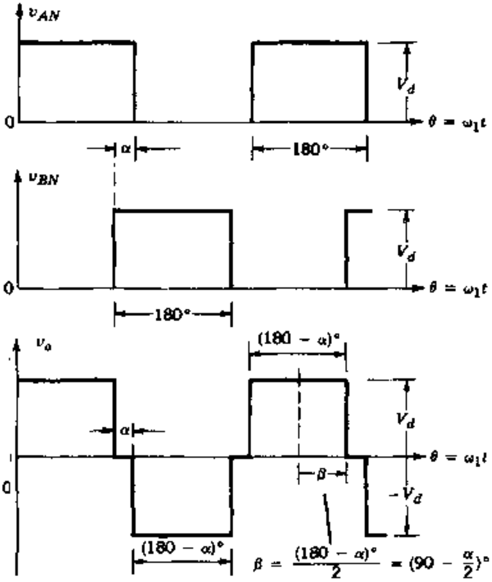
At $h = 2m_f + 1 = 77$ or $3619\ Hz$: $(V_o)_{77} = 0.314 \times 212.13 = 66.60\ V$

Square Wave Operation

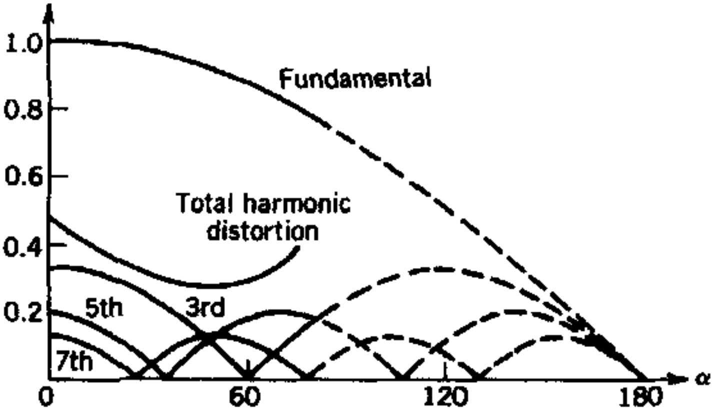
- Full-bridge inverter with **square wave mode of operation**
- Switches (T_{A+}, T_{B-}) and (T_{B+}, T_{A-}) are operated as two pairs with a **duty ratio of 0.5**
- Output voltage magnitude given below is regulated by controlling the input dc voltage

$$\hat{V}_{o1} = \frac{4}{\pi} V_d$$


i_d
+
V_d
−
T_{A+}
D_{A+}
T_{B+}
D_{B+}
i_o
A
+
v_o
B
−
T_{A-}
D_{A-}
T_{B-}
D_{B-}
N


v_{AN}
V_d
0
$\theta = \omega_1 t$
α
180°
v_{BN}
V_d
0
$\theta = \omega_1 t$
180°
v_o
$(180 - \alpha)°$
V_d
α
$\theta = \omega_1 t$
0
β
$-V_d$
$(180 - \alpha)°$
$\beta = \frac{(180 - \alpha)°}{2} = (90 - \frac{\alpha}{2})°$

2.3 Output Control by Voltage Cancellation



2.3 Output Control by Voltage Cancellation

- Feasible only in a single-phase full-bridge inverter
- Based on the combination of square-wave switching and PWM with a unipolar voltage switching
- Switches in the two inverter legs are controlled separately (similar to PWM unipolar voltage switching)
- Also all switches have a duty ratio of 0.5 similar to a square-wave control
- Waveforms for v_{AN} and v_{BN}
- Waveform overlap angle α can be controlled

- During overlap interval, the output voltage is zero
- With $\alpha = 0$, the output waveform is similar to a square-wave inverter with the maximum possible fundamental output magnitude
- $\beta - 90^o - \frac{1}{2}\alpha$

$$(\hat{V}_o)_h = \frac{2}{\pi}\int_{-\pi/2}^{\pi/2} v_o \cos(h\theta)\, d\theta$$

$$= \frac{2}{\pi}\int_{-\beta}^{\beta} V_d \cos(h\theta)\, d\theta$$

$$(\hat{V}_o)_h = \frac{4}{\pi h} V_d \sin(h\beta)$$

2.4 Switch Utilization in Full Bridge Inverters

- Independent of the type of control and the switching scheme used, the peak switch voltage and current ratings required in a full-bridge inverter are

$$V_T = V_d$$
$$I_T = i_{o,\mathrm{peak}}$$

Assumptions :

- $V_{d,max}$ = Highest value of the input voltage
  - PWM mode : Input remains constant at $V_{d,max}$
  - Square-wave mode : Input voltage is decreased below $V_{d,max}$ to decrease the output voltage from its maximum value
- $I_{o,max}$ = RMS value of maximum load current
  - High inductance associated with the output load yields a purely sinusoidal current

2.4 Switch Utilization in Full Bridge Inverters

- Inverter rms volt-ampere (VA) output at fundamental frequency at the maximum rated output $= V_{o1} I_{o,max}$
  - q $=$ Number of switches in inverter
  - V_T $=$ Peak voltage rating of a switch
  - I_T $=$ Peak current rating of a switch

$$\text{Switch utilization ratio} = \frac{V_{o1} I_{o,\max}}{q V_T I_T}$$

- Consider Full bridge inverter with square wave mode of operation at maximum rated output power

$$V_T = V_{d,\max} \qquad I_T = \sqrt{2} I_{o,\max} = \frac{4}{\pi\sqrt{2}} V_{d,\max} \qquad q = 4$$

$$\text{Maximum switch utilization ratio} = \frac{1}{2\pi} \simeq 0.16$$

In practice, switch utilization ratio will be much smaller than 0.16 since

1. Switch ratings are chosen conservatively to provide safety margins
2. In determining the switch rating in a PWM inverter, the variations in the input DC voltage must be considered
3. Ripple in the output current would influence the switch current rating

- At lower output volt-amperes compared to the maximum rated output, switch utilization **decreases linearly**
- For PWM switching with $m_a \leq 1$, switch utilization ratio would be smaller by a factor of $(\pi/4)m_a$ as compared to square wave mode of operation

$$\text{Maximum switch utilization ratio} = \frac{1}{2\pi}\frac{\pi}{4}m_a = \frac{1}{8}m_a \qquad (\text{PWM}, m_a \leq 1.0)$$

- Theoretical maximum switch utilization ratio in a PWM switching is **only 0.125** at $m_a = 1$, as compared with 0.16 in a square wave inverter

Problem

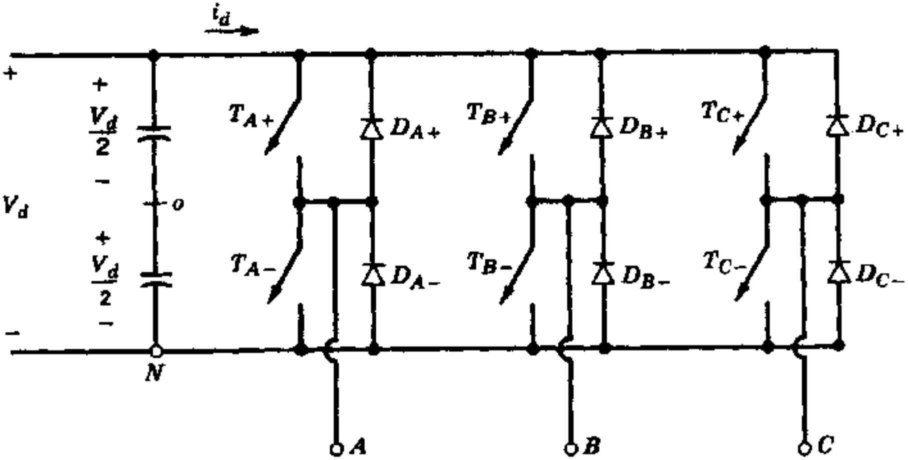
Q) In a single phase full bridge PWM inverter, V_d varies in a range of 295-325 V. The output voltage is requires to be constant at 200 V(rms) and the maximum load current (assumed to be sinusoidal) is 10 A (rms). Calculate the combined switch utilization ratio under idealized conditions.

$$V_T = V_{d,\max} = 325\ V$$
$$I_T = \sqrt{2} I_o = \sqrt{2} \times 10 = 14.14$$
$$q = \text{no. of switches} = 4$$

$$V_{o1} I_{o,\max} = 200 \times 10 = 2000\ \text{VA}$$

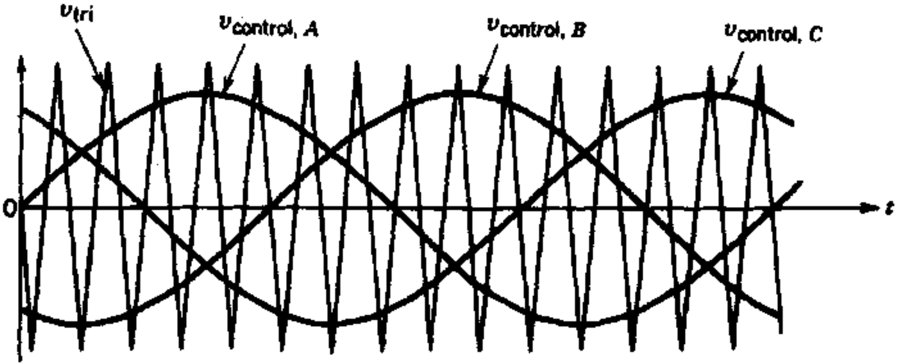
$$\text{Switch utilization ratio} = \frac{V_{o1} I_{o,\max}}{q V_T I_T} = \frac{2000}{4 \times 325 \times 14.14} \simeq 0.11$$

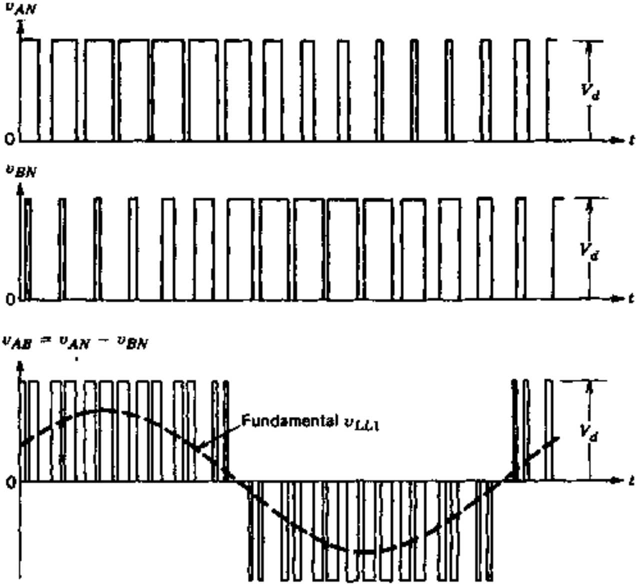
3. 3-phase Voltage Source Inverter



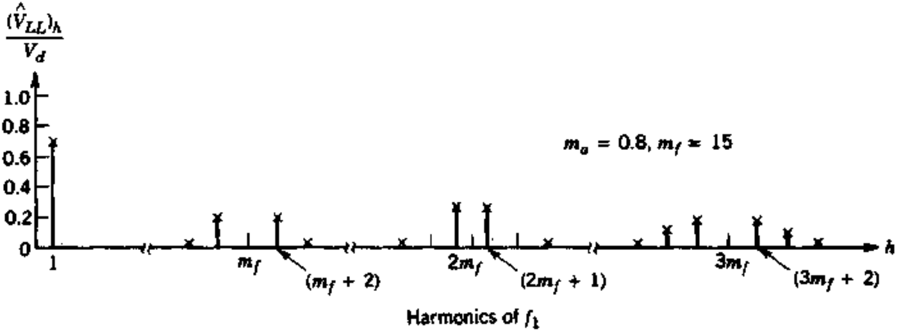
- Three phase inverter consists of three legs $\rightarrow$ one for each phase
- Each inverter leg is similar to basic one leg inverter
- Output of each leg depends only on V_d and switch status
- Output voltage is independent of the output load current since **one of the two switches in a leg is always on at any instant**

3.1 3-phase Sine PWM Inverter




v_{AN}
V_d
0
t
v_{BN}
V_d
0
t
$v_{AB} = v_{AN} - v_{BN}$
Fundamental v_{LL1}
V_d
0
t

3.1 3-phase Sine PWM Inverter



3.1 3-phase Sine PWM Inverter

- Pulse-width-modulated three-phase inverter $\rightarrow$ To shape and control the three-phase output voltages in magnitude and frequency with an essentially constant input voltage V_d
- Same triangular voltage waveform is compared with three sinusoidal control voltages that are 120^o out of phase
- An identical amount of average DC component is present in the output voltages v_{AN}, v_{BN} & v_{CN} and are cancelled out in the line-to-line voltages
- The harmonics in the output of any one of the legs (eg. v_{AN}) are identical to the harmonics in v_{Ao}
    - Only odd harmonics exist as side bands, centred around m_f and its multiples, provided m_f is odd

- Only considering the harmonic at m_f, the phase difference between the m_f harmonic in v_{AN} and v_{BN} is $(120m_f)^o$. This phase difference will be equivalent to zero (a multiple of 360^o) if m_f is odd and a multiple of 3 $\implies$ Harmonic at m_f is suppressed in the line-to-line voltage v_{AB}
- Reason for choosing m_f to be an odd multiple of 3 is to keep m_f odd and hence **eliminate even harmonics**

PWM Scheme

- **For law values of** m_f, to eliminate the even harmonics, a synchronized PWM should be used and m_f should be an odd integer. Moreover, m_f should be a multiple of 3 to cancel out the most dominant harmonics in the line-to-line voltage
- **For large values of** m_f, The amplitudes of sub-harmonics due to asynchronous PWM are small at large values of m_f. Hence asynchronous PWM can be used where the frequency of the triangular waveform is kept constant, whereas the frequency of $v_{control}$ varies, resulting in non-integer values of m_f
- **During over-modulation** $(m_a > 1)$, regardless of the value of m_f, synchronized PWM must be used

Linear Modulation ($m_a \leq 1.0$)

- In the linear region, the fundamental-frequency component in the output voltage varies **linearly** with the amplitude modulation ratio m_a
- Peak value of the fundamental-frequency component in one of the inverter legs,

$$(\hat{V}_{AN})_1 = m_a \frac{V_d}{2}$$

- **Line-to-line rms voltage at the fundamental frequency**, due to 120^o phase displacement between phase voltages,

$$\underset{\text{(line–line, rms)}}{V_{LL_1}} = \frac{\sqrt{3}}{\sqrt{2}}(\hat{V}_{AN})_1 = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d \simeq 0.612 m_a V_d$$

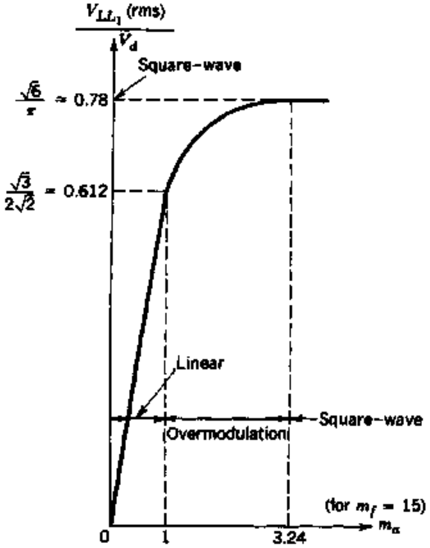
- RMS harmonic voltages of Line to Line output voltages,

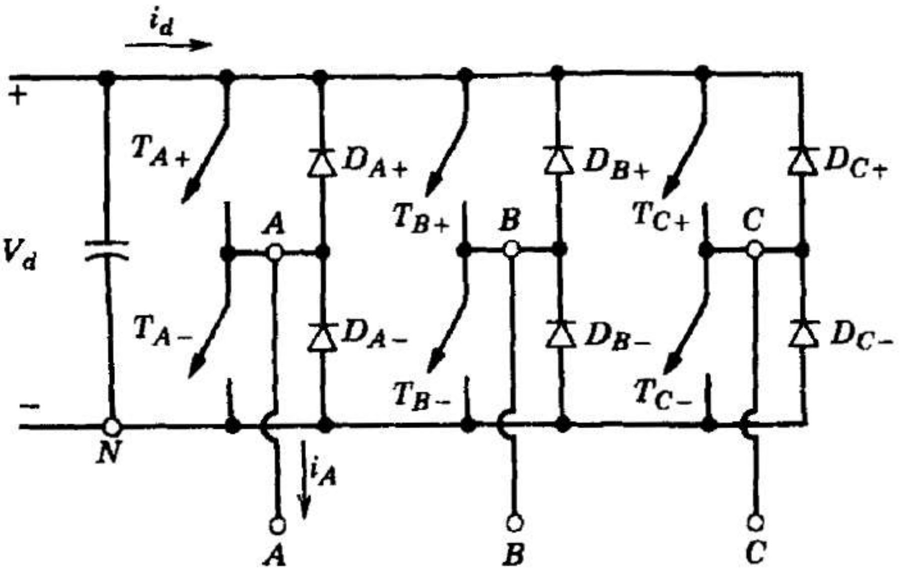
h \ m_a	0.2	0.4	0.6	0.8	1.0
1	0.122	0.245	0.367	0.490	0.612
$m_f \pm 2$	0.010	0.037	0.080	0.135	0.195
$m_f \pm 4$				0.005	0.011
$2m_f \pm 1$	0.116	0.200	0.227	0.192	0.111
$2m_f \pm 5$				0.008	0.020
$3m_f \pm 2$	0.027	0.085	0.124	0.108	0.038
$3m_f \pm 4$		0.007	0.029	0.064	0.096
$4m_f \pm 1$	0.100	0.096	0.005	0.064	0.042
$4m_f \pm 5$			0.021	0.051	0.073
$4m_f \pm 7$				0.010	0.030

Over-modulation ($m_a > 1.0$)

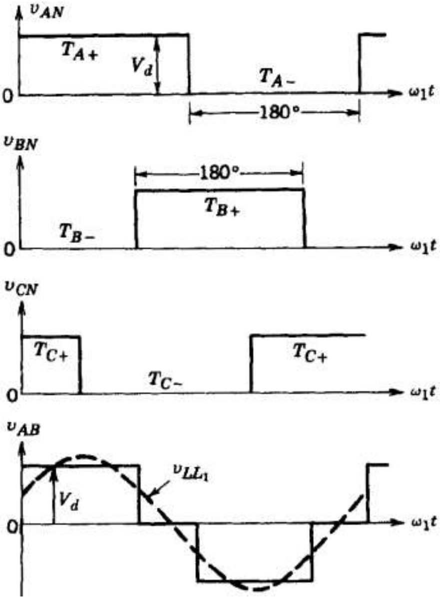
- Fundamental frequency voltage magnitude does not increase proportionally with m_a
- For sufficiently large values of m_a, the PWM degenerates into a square-wave inverter waveform $\implies$ Maximum value of $V_{LL1} = 0.78V_d$
- In the over-modulation region, more side-band harmonics appear centred around the frequencies of harmonics m_f and its multiples
- Dominant harmonics may not have as large an amplitude as with $m_a \leq 1 \rightarrow$ Power loss in the load due to the harmonic frequencies may not be as high in the over-modulation region

Over-modulation ($m_a > 1.0$)

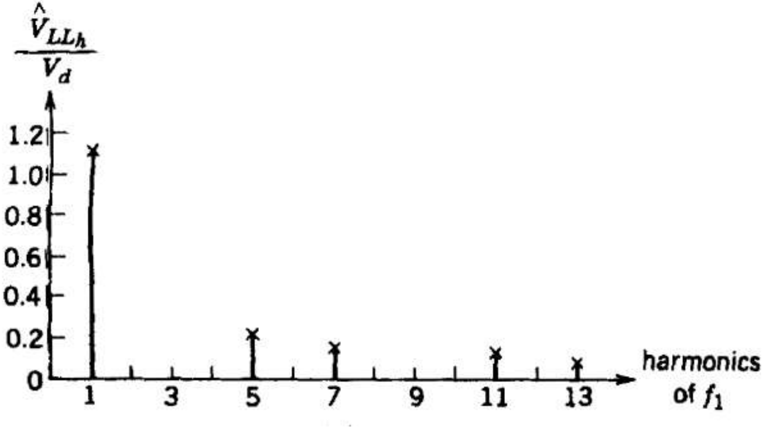




i_d
+
V_d
−
N
T_{A+}
D_{A+}
T_{A-}
D_{A-}
T_{B+}
D_{B+}
T_{B-}
D_{B-}
T_{C+}
D_{C+}
T_{C-}
D_{C-}
A
B
C
i_A
A
B
C



v_{AN}
T_{A+}
V_d
T_{A-}
0
$\omega_1 t$
180°
v_{BN}
180°
T_{B+}
T_{B-}
0
$\omega_1 t$
v_{CN}
T_{C+}
T_{C-}
T_{C+}
0
$\omega_1 t$
v_{AB}
v_{LL_1}
V_d
0
$\omega_1 t$


$\frac{\hat{V}_{LLh}}{V_d}$
1.2
1.0
0.8
0.6
0.4
0.2
0
1
3
5
7
9
11
13
harmonics of f_1

- If the input DC voltage V_d is controllable, the inverter can be operated in a square-wave mode
- For sufficiently large values of m_a, PWM degenerates into square-wave operation
- Each switch is ON for 180^o (ie, D = 0.5)
- At any instant of time, three switches are ON
- DC input voltage must be controlled in order to control the output voltage magnitude
- Fundamental frequency line-to-line rms output voltage

$$\underset{(\mathrm{rms})}{V_{LL_1}} = \frac{\sqrt{3}}{\sqrt{2}} \frac{4}{\pi} \frac{V_d}{2} = \frac{\sqrt{6}}{\pi} V_d \simeq 0.78 V_d$$

- Line-to-line output voltage waveform does not depend on the load
- Line-to-line output voltage contains harmonics ($6n \pm 1; n = 1, 2, ..$), whose amplitudes decrease inversely proportional to their harmonic order

$$V_{LL_h} = \frac{0.78}{h} V_d$$

$$h = 6n \pm 1 \qquad (n = 1, 2, 3, \ldots)$$

- It is **not possible** to control the output voltage magnitude in a three-phase square-wave inverter by means of **voltage cancellation technique**

3.3 Switch Utilization in 3-phase Inverter

- $V_{d,max}$ = Highest value of the input voltage
  - PWM mode : Input remains constant at $V_{d,max}$
  - Square-wave mode : Input voltage is decreased below $V_{d,max}$ to decrease the output voltage from its maximum value
- $I_{o,max}$ = RMS value of maximum load current
  - High inductance associated with the output load yields a purely sinusoidal current
- Peak voltage and current ratings of switch

$$V_T = V_{d,\max}$$

$$I_T = \sqrt{2} I_{o,\max}$$

- V_{LL1} = RMS value of the fundamental frequency line-to-line output voltage
- Three-phase output volt-amperes (rms) at the fundamental frequency at the rated output,

$$(\mathrm{VA})_{\text{3-phase}} = \sqrt{3} V_{LL_1} I_{o,\max}$$

- Total switch utilization ratio of all six switches combined,

$$\text{Switch utilization ratio} = \frac{(\mathrm{VA})_{3\text{-phase}}}{6V_T I_T}$$

$$= \frac{\sqrt{3}V_{LL_1} I_{o,\max}}{6V_{d,\max}\sqrt{2}I_{o,\max}}$$

$$= \frac{1}{2\sqrt{6}}\frac{V_{LL_1}}{V_{d,\max}}$$

- In PWM linear region ($m_a \leq 1$), maximum switch utilization occurs at $V_d = V_{d,max}$

$$\text{Maximum switch utilization ratio (PWM)} = \frac{1}{2\sqrt{6}} \frac{\sqrt{3}}{2\sqrt{2}} m_a$$

$$= \frac{1}{8} m_a \qquad (m_a \leq 1.0)$$

- In the square-wave mode, maximum switch utilization ratio is $(1/2\pi)$ $= 0.16$ compared to a maximum of 0.125 for a PWM linear region with $m_a = 1.0$
- The maximum switch utilization ratio is the same in a three-phase, three-leg inverter as in a single-phase inverter
- Using the switches with identical ratings, a three-phase inverter with 50% increase in the number of switches results in a 50% increase in the output volt-ampere, compared to a single-phase inverter

References

1. Mohan, Undeland, Robbins, *"Power Electronics Converters Application and Design"*, Wiley-India
2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

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Switched Mode Power Converters

(EE364)

S6-EEE

by

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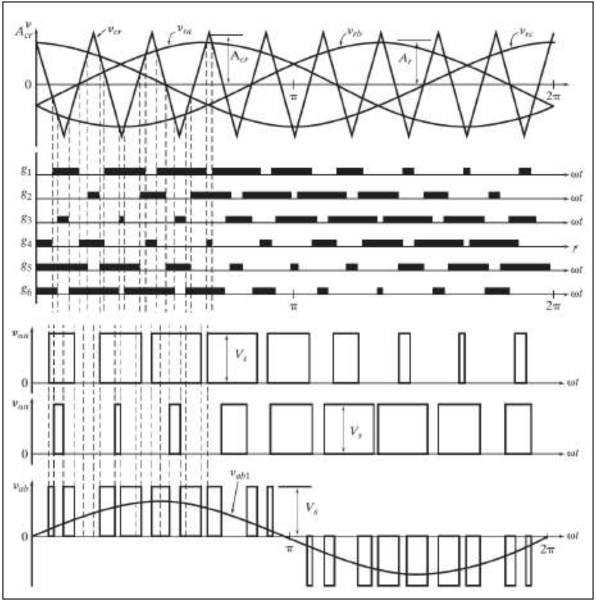
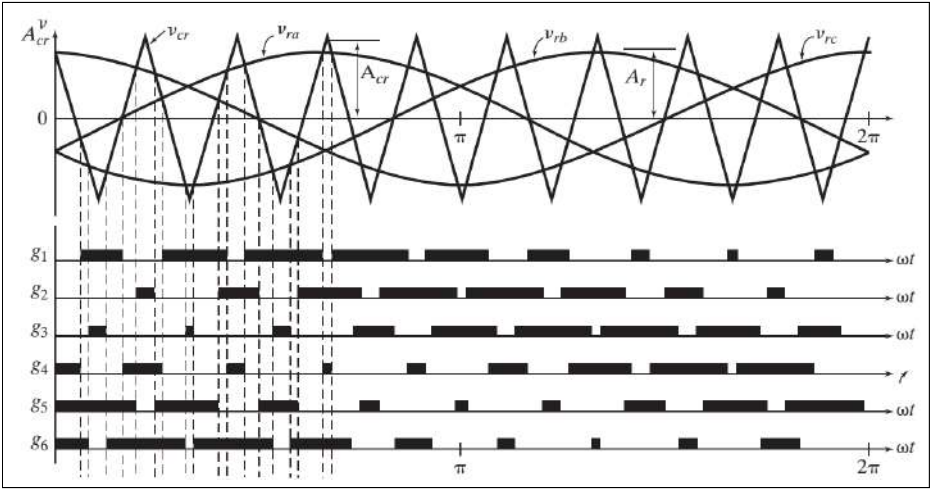
Module 5 - Overview

- Voltage Control Techniques
  - **Sinusoidal PWM**
    - Commonly used
    - Peak amplitude of the output voltage cannot exceed the DC supply voltage (V_S) without operation in the over-modulation region
  - Third-harmonic PWM
    - Gives limited AC output voltage control
  - 60^o PWM
    - Gives the fundamental component, which is higher than the available supply (V_S)
  - **Space Vector Modulation**
    - More flexible
    - It can be programmed to synthesize the output voltage with a digital implementation

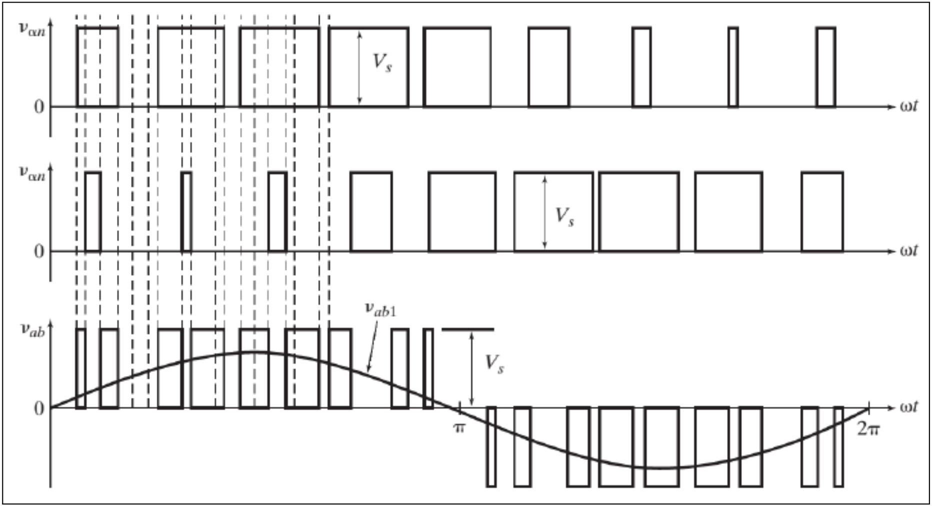


A_{cr}
v
v_{cr}
v_{ra}
v_{rb}
v_{rc}
A_{cr}
A_r
0
π
2π
g_1
g_2
g_3
g_4
g_5
g_6
ωt
v_{an}
V_s
v_{bn}
v_{ab}
v_{ab1}

2. Sinusoidal PWM



2. Sinusoidal PWM



2. Sinusoidal PWM

- Gating signals are generated with sinusoidal PWM
- Three sinusoidal reference waves (v_{ra}, v_{rb}, v_{rc}) each shifted by 120^o
- Carrier wave (v_{cr}) is compared with each reference signal to generate the gating signals (g_1, g_3, g_5 etc.) for that phase
- When $v_{ra} > v_{cr}$, the upper switch Q_1 in inverter leg a is turned ON
- Lower switch Q_4 is complementary to $Q_1 \implies$ Two switching devices in the same arm cannot conduct at the same time
- $v_{an} = V_S * g_1$
- $v_{bn} = V_S * g_3$
- Instantaneous line-to-line output voltage, $v_{ab} = V_s(g_1 - g_3)$
- Fundamental component of the lineline voltage $v_{ab} = v_{ab1}$

- Normalized carrier frequency m_f should be an odd multiple of three
  - $\Longrightarrow$ All phase voltages (v_{aN}, v_{bN}, v_{cN}) are identical, but 120^o out of phase without even harmonics
  - Harmonics at frequencies of multiples of three are identical in amplitude and phase in all phases

$$v_{aN9}(t) = \hat{v}_9 \sin(9\omega t)$$

$$\begin{aligned} v_{bN9}(t) &= \hat{v}_9 \sin(9(\omega t - 120^\circ)) \\ &= \hat{v}_9 \sin(9\omega t - 1080^\circ)) \\ &= \hat{v}_9 \sin(9\omega t) \end{aligned}$$

  - $\therefore$ AC output line voltage $v_{ab} = v_{aN} - v_{bN}$ does not contain the ninth harmonic
  - For odd multiples of three times the normalized carrier frequency m_f, the harmonics in the AC output voltage appear at normalized frequencies f_h centred around m_f and its multiples, specifically, at $n = jm_f \pm k$ where j = 1,3,5..... for k = 2,4,6...... and j = 2,4,6........ for k = 1,3,5..... such that n is not a multiple of three

- Hence harmonics are at $m_f \pm 2$, $m_f \pm 4$......, $2m_f \pm 1$, $2m_f \pm 5$,.........., $3m_f \pm 2$, $3m_f \pm 4$,........, $4m_f \pm 1$, $4m_f \pm 5$,........
- For nearly sinusoidal AC load current, the harmonics in the DC-link current are at frequencies $n = jm_f \pm k \pm 1$ where j = 0,2,4.... for k = 1,5,7..... and j = 1,3,5...... for k = 2,4,6.... such that $n = jm_f \pm k$ is positive and not a multiple of three
- Maximum amplitude of the fundamental phase voltage in the linear region $(M \leq 1)$ is $V_s/2$
- Maximum amplitude of the fundamental ac output line voltage,
$$\hat{v_{ab1}} = \sqrt{3}V_s/2$$
- Therefore peak amplitude

$$\hat{v}_{ab1} = M\sqrt{3}\frac{V_s}{2} \quad \text{for } 0 < M \leq 1$$

Over-modulation

- To further increase the amplitude of the load voltage, the amplitude of the modulating signal $\hat{v}_r$ can be made higher than the amplitude of the carrier signal $\hat{v_{cr}}$
- Relationship between the amplitude of the fundamental AC output line voltage and the DC-link voltage becomes non-linear

$$\sqrt{3}\,\frac{V_s}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi}\sqrt{3}\,\frac{V_s}{2}$$

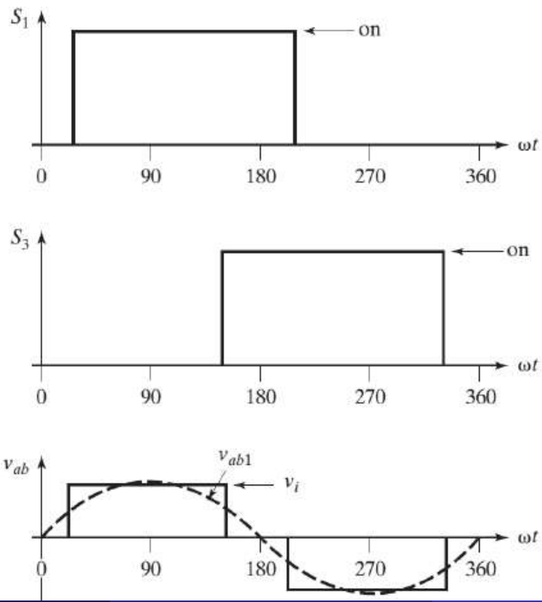
- Large values of M in the SPWM technique lead to full over-modulation $\Longrightarrow$ **Square-wave operation**
    - Power devices are ON for 180^o
    - Inverter cannot vary the load voltage except by varying the DC supply voltage V_s
    - Fundamental AC line voltage

$$\hat{v}_{ab1} = \frac{4}{\pi}\sqrt{3}\,\frac{V_s}{2}$$

- AC line output voltage contains the harmonics f_n, where $n = 6k \pm 1$ (k = 1,2,3....) and their amplitudes are inversely proportional to their harmonic order n

$$\hat{v}_{abn} = \frac{1}{n}\,\frac{4}{\pi}\sqrt{3}\,\frac{V_s}{2}$$

Square-wave Operation



Problem

Q) A single-phase full-bridge inverter controls the power in a resistive load. The nominal value of input DC voltage is $V_s = 220$ V and a uniform pulse-width modulation with five pulses per half cycle is used. For the required control, the width of each pulse is 30^o.
(a) Determine the rms voltage of the load.
(b) If the DC supply increases by 10%, determine the pulse width to maintain the same load power. If the maximum possible pulse width is 35^o, determine the minimum allowable limit of the DC input source

Problem

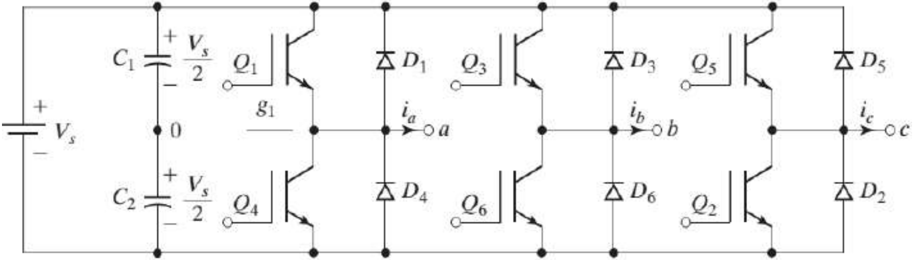
Q) A single-phase full-bridge inverter controls the power in a resistive load. The nominal value of input DC voltage is $V_s = 220$ V and a uniform pulse-width modulation with five pulses per half cycle is used. For the required control, the width of each pulse is 30^o.
(a) Determine the rms voltage of the load.
(b) If the DC supply increases by 10%, determine the pulse width to maintain the same load power. If the maximum possible pulse width is 35^o, determine the minimum allowable limit of the DC input source

a. $V_s = 220\,V$, $p = 5$, and $\delta = 30°$. From Eq. (6.31), $V_o = 220\sqrt{5 \times 30/180} = 200.8\,\text{V}$.

b. $V_s = 1.1 \times 220 = 242\,\text{V}$. By using Eq. (6.31), $242\sqrt{5\delta/180} = 200.8$ and this gives the required value of pulse width, $\delta = 24.75°$.

To maintain the output voltage of 200.8 V at the maximum possible pulse width of $\delta = 35°$, the input voltage can be found from $200.8 = V_s\sqrt{5 \times 35/180}$, and this yields the minimum allowable input voltage, $V_s = 203.64\,\text{V}$.

3. Space Vector Modulation (SVM)



3. Space Vector Modulation (SVM)

Switch States for Three-Phase Voltage-Source Inverter

State	State No.	Switch States	v_{ab}	v_{bc}	v_{ca}	Space Vector
S_1, S_2, and S_6 are on and S_4, S_5, and S_3 are off	1	100	V_S	0	$-V_S$	$\mathbf{V}_1 = 1 + j0.577 = 2/\sqrt{3}\ \angle 30°$
S_2, S_3, and S_1 are on and S_5, S_6, and S_4 are off	2	110	0	V_S	$-V_S$	$\mathbf{V}_2 = j1.155 = 2/\sqrt{3}\ \angle 90°$
S_3, S_4, and S_2 are on and S_6, S_1, and S_5 are off	3	010	$-V_S$	V_S	0	$\mathbf{V}_3 = -1 + j0.577 = 2/\sqrt{3}\ \angle 150°$
S_4, S_5, and S_3 are on and S_1, S_2, and S_6 are off	4	011	$-V_S$	0	V_S	$\mathbf{V}_4 = -1 - j0.577 = 2/\sqrt{3}\ \angle 210°$
S_5, S_6, and S_4 are on and S_2, S_3, and S_1 are off	5	001	0	$-V_S$	V_S	$\mathbf{V}_5 = -j1.155 = 2/\sqrt{3}\ \angle 270°$
S_6, S_1, and S_5 are on and S_3, S_4, and S_2 are off	6	101	V_S	$-V_S$	0	$\mathbf{V}_6 = 1 - j0.577 = 2/\sqrt{3}\ \angle 330°$
S_1, S_3, and S_5 are on and S_4, S_6, and S_2 are off	7	111	0	0	0	$\mathbf{V}_7 = 0$
S_4, S_6, and S_2 are on and S_1, S_3, and S_5 are off	8	000	0	0	0	$\mathbf{V}_0 = 0$

3. Space Vector Modulation (SVM)

- SVM treats the inverter as a single unit
- Inverter can be driven to eight unique states
- Modulation is accomplished by switching the state of the inverter
- Control strategies are implemented in digital systems
- SVM is a digital modulating technique where the objective is to generate PWM load line voltages that are in average equal to a given (or reference) load line voltage. This is done in each sampling period by properly selecting the switch states of the inverter and the calculation of the appropriate time period for each state. The selection of the states and their time periods are accomplished by the space vector (SV) transformation

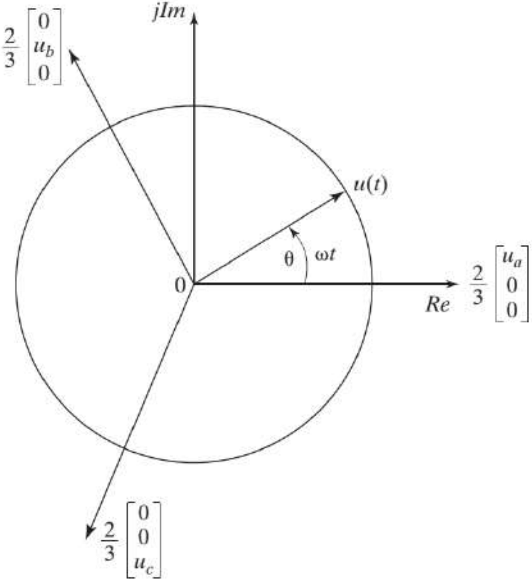
Space Transformation

- **Any three functions of time that satisfy $u_a(t) + u_b(t) + u_c(t) = 0$ can be represented in a two-dimensional stationary space**
- $u_c(t) = -u_a(t) - u_b(t)$
- abc/xy transformation $\rightarrow$ Transformation of three-phase variables to two-phase variables
- A rotating space vector(s) u(t) in complex notation,

$$\mathbf{u}(t) = \frac{2}{3}[u_a + u_b e^{j(2/3)\pi} + u_c e^{-j(2/3)\pi}]$$

- The real and imaginary components in the xy domain,

$$\mathbf{u}(t) = u_x + j u_y$$



jIm
$\frac{2}{3}\begin{bmatrix}0\\u_b\\0\end{bmatrix}$
$u(t)$
θ
ωt
0
Re
$\frac{2}{3}\begin{bmatrix}u_a\\0\\0\end{bmatrix}$
$\frac{2}{3}\begin{bmatrix}0\\0\\u_c\end{bmatrix}$

- Coordinate transformation from the abc-axis to the xy axis

$$\begin{pmatrix} u_x \\ u_y \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}$$

$$u_x = \frac{2}{3} [v_a - 0.5(v_b + v_c)]$$

$$u_y = \frac{\sqrt{3}}{3}(v_b - v_c)$$

- The transformation from the xy axis to the $\alpha - \beta$ axis, which is rotating with an angular velocity of ω, can be obtained by rotating the xy-axis with ωt as given by

$$\begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} = \begin{pmatrix} \cos(\omega t) & \cos\left(\frac{\pi}{2} + \omega t\right) \\ \sin(\omega t) & \sin\left(\frac{\pi}{2} + \omega t\right) \end{pmatrix} \begin{pmatrix} u_x \\ u_y \end{pmatrix}$$

$$= \begin{pmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{pmatrix} \begin{pmatrix} u_x \\ u_y \end{pmatrix}$$

- Inverse transformation

$$u_a = \mathrm{Re}(\mathbf{u})$$
$$u_b = \mathrm{Re}(\mathbf{u}e^{-j(2/3)\pi})$$
$$u_c = \mathrm{Re}(\mathbf{u}e^{j(2/3)\pi})$$

3. Space Vector Modulation (SVM)

- If u_a, u_b and u_c are the three-phase voltages of a balanced supply with a peak value of V_m, then

$$u_a = V_m \cos(\omega t)$$
$$u_b = V_m \cos(\omega t - 2\pi/3)$$
$$u_c = V_m \cos(\omega t + 2\pi/3)$$

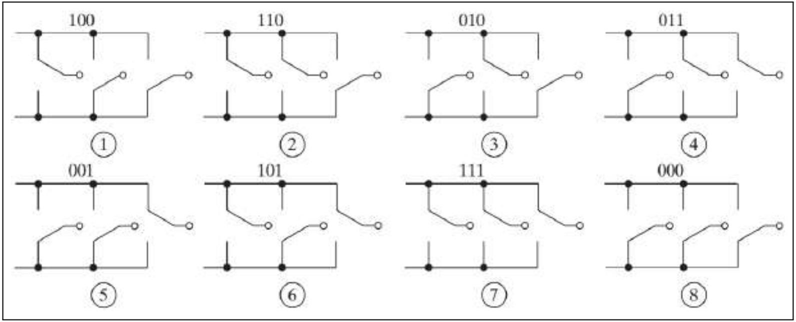
- **Space Vector** representation

$$\mathbf{u}(t) = V_m e^{j\theta} = V_m e^{j\omega t}$$

- Space vector is a vector of magnitude V_m rotating at a constant speed ω in radians per second

3.1 Concept of Space Vector

- Switching states of the inverter can be represented by binary values q_1, q_2, q_3, q_4, q_5 and q_6
  - $q_k = 1$ when a switch is turned ON
  - $q_k = 0$ when a switch is turned OFF
- Pairs $(q_1 q_4), (q_3 q_6)$ and $(q_5 q_2)$ are complementary
  - $q_4 = 1 - q_1$
  - $q_6 = 1 - q_3$
  - $q_2 = 1 - q_5$



3.1 Concept of Space Vector

- $e^{j\theta} = cos\theta + \text{j } sin\theta \qquad$ for $\theta = 0, 2\pi/3$ or $4\pi/3$
- Output phase voltage in the switching state (100)

$$v_a(t) = \frac{2}{3}V_S; \quad v_b(t) = \frac{-1}{3}V_S; \quad v_c(t) = \frac{-1}{3}V_S$$

- Space vector V_1 corresponding to the switching state (100)

$$\mathbf{V_1} = \frac{2}{3}V_S e^{j0}$$

- In general

$$\mathbf{V_n} = \frac{2}{3}V_S e^{j(n-1)\frac{\pi}{3}} \quad \text{for } n = 1, 2, \ldots 6$$

- Zero-vector has two switching states (111) and (000) $\implies$ one redundant state
- Redundant switching state can be utilized to optimize the operation of the inverter such as minimizing the switching frequency
- Space vectors do not move in space $\implies$ stationary vectors
- Vector u(t) rotates at an angular velocity of $\omega = 2\pi f$
  where f is the fundamental frequency of the inverter output voltage
- Three-phase to two-phase transformation

$$\begin{pmatrix} V_{L\alpha} \\ V_{L\beta} \end{pmatrix} = \frac{2}{3}\sqrt{\frac{3}{2}} V_s \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} q_1 \\ q_3 \\ q_5 \end{pmatrix}$$

- Peak value of line voltage, $V_{L(peak)} = 2V_S/\sqrt{3}$
- Peak value of phase voltage, $V_{p(peak)} = V_S/\sqrt{3}$
- Line voltage vector V_{ab} leads the phase vector by $\pi/6$

3.1 Concept of Space Vector

- Normalized peak value of n_{th} line voltage vector,

$$\mathbf{V_n} = \frac{\sqrt{2} \times \sqrt{2}}{\sqrt{3}} e^{j(2n-1)\pi/6} = \frac{2}{\sqrt{3}}\left[\cos\left(\frac{(2n-1)\pi}{6}\right) + j\sin\left(\frac{(2n-1)\pi}{6}\right)\right]$$

$$\text{for } n = 0, 1, 2, 6$$

- Six **non-zero vectors**, (V_1 to V_6) and two **zero vectors**, (V_0 and V_7)
- Performance vector U as the time integral function of V_n

$$\mathbf{U} = \int \mathbf{V_n}\, dt + \mathbf{U_0}$$

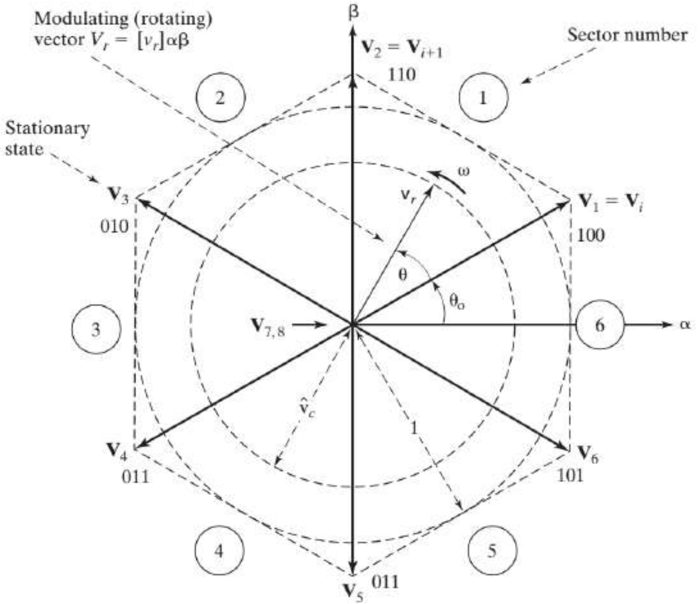
where U_0 is the initial condition

- U draws a hexagon locus that is determined by the magnitude and the time period of voltage vectors
- If output voltages are purely sinusoidal, then performance vector U,

$$\mathbf{U}^* = Me^{j\theta} = Me^{j\omega t}$$

where M $=$ modulation index $0 < M < 1$ and

$\omega =$ output frequency in radians per second


Modulating (rotating) vector $V_r = [v_r]\alpha\beta$
Sector number
Stationary state
β
$\mathbf{V}_2 = \mathbf{V}_{i+1}$
110
$\mathbf{V}_1 = \mathbf{V}_i$
100
$\mathbf{V}_3$
010
$\mathbf{V}_4$
011
$\mathbf{V}_5$
011
$\mathbf{V}_6$
101
$\mathbf{V}_{7,8}$
$\mathbf{v}_r$
ω
θ
θ_o
$\hat{v}_c$
1
α
1
2
3
4
5
6

- U^* draws a pure circle locus of radius M=1 $\implies$ Reference vector V_r
- Locus U can be controlled by selecting V_n and adjusting the time width of V_n to follow the U^* locus as closely as possible $\implies$ **Quasi-circular Locus Method**
- Angular displacement between reference vector V_r and α of the $\alpha - \beta$ frame can be obtained by

$$\theta(t) = \int_0^t \omega(t)\,dt + \theta_o$$

- When the reference (or modulating) vector V_r passes through the sectors one by one, different sets of switches will be turned ON or OFF according to the switching states
- When V_r rotates one revolution in space, the inverter output voltage completes one cycle over time
- Inverter output frequency corresponds to the rotating speed of V_r and its output voltage can be adjusted by varying the magnitude of V_r

3.2 Modulating Reference Vector

- Vectors of three-phase line modulating signals $[v_r]_{abc} = [v_{ra}\ v_{rb}\ v_{rc}]^T$ can be represented by the complex vector
  $U^* = V_r = [v_r]_{\alpha\beta} = [v_{r\alpha}\ v_{r\beta}]^T$ as given by

$$v_{r\alpha} = \frac{2}{3}[v_{ra} - 0.5(v_{rb} + v_{cr})]$$
$$v_{r\beta} = \frac{\sqrt{3}}{3}(v_{rb} - v_{rc})$$

- If the line modulating signals $[v_r]_{abc}$ are three balanced sinusoidal waveforms with an amplitude of $A_c = 1$ and an angular frequency ω, the resulting modulating signals in the $\alpha - \beta$ stationary frame $V_c = [v_r]_{\alpha\beta}$ becomes a vector of fixed amplitude $MA_c(= M)$ that rotates at frequency ω

3.3 Switching Times

- Reference vector V_r in a particular sector can be synthesized to produce a given magnitude and position from the three nearby stationary space vectors and the gating signals for the switching devices in each sector can also be generated
- Objective of the SV switching is to approximate the sinusoidal line modulating signal V_r with the eight space vectors $(V_n, n = 0, 2, ..., 7)$

3.3 Switching Times

- If the modulating signal V_r is laying between the arbitrary vectors V_n and V_{n+1}, then the two non-zero vectors (V_n and V_{n+1}) and one zero SV ($V_z = V_0$ or V_7) should be used to obtain the maximum load line voltage and to minimize the switching frequency
  - A voltage vector V_r in section 1 can be realized by the V_1 and V_2 vectors and one of the two null vectors (V_0 or V_7)
  - V_1 state is active for time T_1, V_2 is active for T_2 and one of the null vectors (V_0 or V_7) is active for T_z
  - For a sufficiently high-switching frequency, the reference vector V_r can be assumed constant during one switching period
  - Since the vectors V_1 and V_2 are constant and $V_z = 0$, we can equate the volt-time of the reference vector to the SVs as

$$\mathbf{V_r} \times T_s = \mathbf{V_1} \times T_1 + \mathbf{V_2} \times T_2 + \mathbf{V_z} \times T_z$$

$$T_s = T_1 + T_2 + T_z$$

  - T_1, T_2 and T_z are the dwell times for vectors V_1, V_2 and V_z respectively

- space vectors in sector 1

$$\mathbf{V_1} = \frac{2}{3}V_S; \quad \mathbf{V_2} = \frac{2}{3}V_S e^{j\frac{\pi}{3}}; \quad \mathbf{V_z} = 0; \quad \mathbf{V_r} = V_r e^{j\theta}$$

  where V_r is the magnitude of the reference vector and θ is the angle of V_r

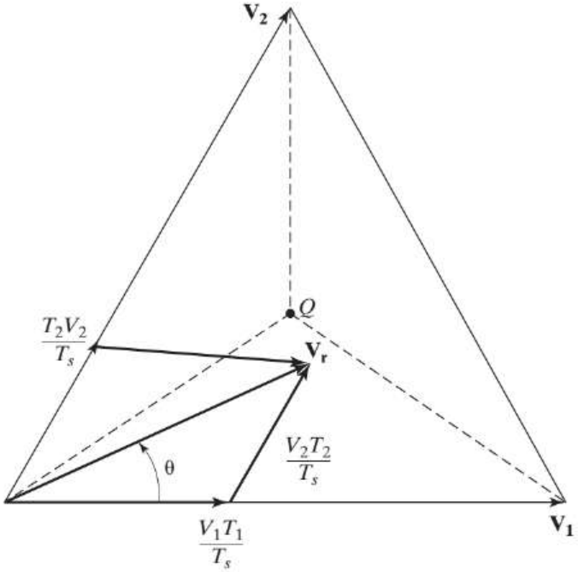
- V_r can be generated by using two adjacent SVs with the appropriate duty cycle as shown in figure

$$T_s V_r e^{j\theta} = T_1 \frac{2}{3} V_S + T_2 \frac{2}{3} V_S e^{j\frac{\pi}{3}} + T_z \times 0$$

- In rectangular coordinates

$$T_s V_r (\cos\theta + j\sin\theta) = T_1 \frac{2}{3} V_S + T_2 \frac{2}{3} V_s\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right) + T_z \times 0$$

3.3 Switching Times



- Equating the real and imaginary parts on both sides

$$T_s V_r \cos\theta = T_1 \frac{2}{3} V_S + T_2 \frac{2}{3} V_S \cos\frac{\pi}{3} + T_z \times 0$$

$$jT_s V_r \sin\theta = jT_2 \frac{2}{3} V_S \sin\frac{\pi}{3}$$

- Solving for T_1, T_2 and T_z in sector 1 $(0 \leq \theta \leq \pi/3)$

$$T_1 = \frac{\sqrt{3}\, T_s V_r}{V_S} \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_2 = \frac{\sqrt{3}\, T_s V_r}{V_S} \sin(\theta)$$

$$T_z = T_s - T_1 - T_2$$

- If V_r lies in the middle of vector V_1 and V_2 so that $\theta = \pi/6$, then the dwell time $T_1 = T_2$
- If V_r is closer to V_2, then $T_2 > T_1$
- If V_r is aligned in the direction of the central point, then the dwell time $T_1 = T_2 = T_z$
- For k^{th} sector, $\theta \to \theta_k$

$$\theta_k = \theta - (k-1)\frac{\pi}{3} \quad \text{for } 0 \leq \theta_k \leq \pi/3$$

Modulation Index

- Modulation Index

$$M = \frac{\sqrt{3}\,V_r}{V_S}$$

- Dwell Times

$$T_1 = T_s M \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_2 = T_s M \sin(\theta)$$

$$T_z = T_s - T_1 - T_2$$

Relationship between the Dwell Times and the Space Vector Angle θ for Sector 1

Angle	$\theta = 0$	$0 \le \theta \le \pi/6$	$\theta = \pi/6$	$0 \le \theta \le \pi/3$	$\theta = \pi/3$
Dwell time T_1	$T_1 > 0$	$T_1 > T_2$	$T_1 = T_2$	$T_1 < T_2$	$T_1 = 0$
Dwell time T_2	$T_2 = 0$	$T_2 < T_1$	$T_1 = T_2$	$T_2 > T_1$	$T_2 > 0$

Modulation Index

- Let
  - V_{a1} = RMS value of the fundamental component of the inverter output phase (phase-a) voltage
  - V_r = Peak reference value

$$V_r = \sqrt{2} V_{a1}$$

$\Longrightarrow$

$$M = \frac{\sqrt{3}\, V_r}{V_S} = \frac{\sqrt{6}\, V_{a1}}{V_S}$$

- $\Longrightarrow$ **RMS output voltage (V_{a1}) is proportional to the modulation index** (M)
- In SVM, hexagon is formed by six stationary vectors having a length of $2V_S/3$, the maximum value of the reference vector is given by

$$V_{r(\max)} = \frac{2}{3} V_S \times \frac{\sqrt{3}}{2} = \frac{V_S}{\sqrt{3}}$$

Modulation Index

- Maximum modulation index M_{max}

$$M_{\max} = \frac{\sqrt{3}}{V_S} \times \frac{V_S}{\sqrt{3}} = 1$$

- Range of the modulation index for SVM

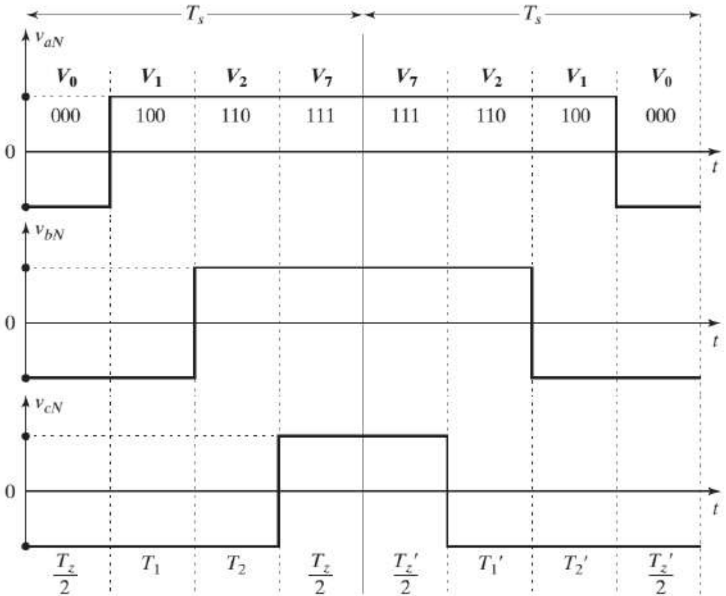
$$0 \leq M_{\max} \leq 1$$

3.4 Space Vector Sequence

- SV sequence should assure that the load line voltages have the quarter-wave symmetry to reduce even harmonics in their spectra
- To reduce the switching frequency, it is also necessary to arrange the switching sequence in such a way that the transition from one to the next is performed by switching only one inverter leg at a time
- The transition for moving from one sector in the space vector diagram to the next requires no or a minimum number of switching
- These conditions are met by the sequence $V_z, V_n, V_{n+1} Vz$ (where V_z is alternately chosen between V_0 and V_7)

- If V_r falls in section 1, the switching sequence is $V_0, V_1, V_2, V_7, V_2, V_1, V_0$
- $T_z (= T_0 = T_7)$ can be split and distributed at the beginning and at the end of the sampling period T_s
- In general, the time intervals of the null vectors are equally distributed with $T_z/2$ at the beginning and $T_z/2$ at the end

3.4 Space Vector Sequence



3.4 Space Vector Sequence

SVM pattern has the following characteristics

- The SVM pattern has a quarter-wave symmetry
- The dwell times for the seven segments add up to the sampling period ($T_s = T_1 + T_2 + T_z$) or a multiple of T_s
- The transition from state (000) to state (100) involves only two switches and is accomplished by turning Q_1 ON and Q_4 OFF
- The switching state (111) is selected for the $T_z/2$ segment in the centre to reduce the number of switching per sampling period. The switching state (000) is selected for the $T_z/2$ segments on both sides
- Each of the switches in the inverter turns ON and OFF once per sampling period. The switching frequency f_{sw} of the devices is thus equal to the sampling frequency $f_s = 1/T_s$ or its multiple
- The pattern of waveform can be produced for a duration of nT_s that is a multiple (n) or a fraction (1/n) of the sampling period T_s by either multiplying or dividing the dwell times by n. ie, if we multiply by 2, the segments will cover two sampling periods

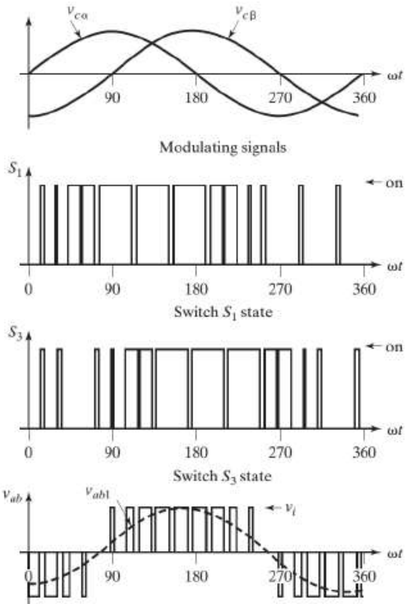
- Instantaneous phase voltages can be found by time averaging of the SVs during one switching period for sector 1

$$v_{aN} = \frac{V_s}{2T_s}\left(\frac{-T_z}{2} + T_1 + T_2 + \frac{T_z}{2}\right) = \frac{V_s}{2}\sin\left(\frac{\pi}{3} + \theta\right)$$

$$v_{bN} = \frac{V_s}{2T_s}\left(\frac{-T_z}{2} - T_1 + T_2 + \frac{T_z}{2}\right) = V_s\frac{\sqrt{3}}{2}\sin\left(\theta - \frac{\pi}{6}\right)$$

$$v_{cN} = \frac{V_s}{T_s}\left(\frac{-T_z}{2} - T_1 - T_2 + \frac{T_z}{2}\right) = -V_{aN}$$

- To minimize uncharacteristic harmonics in SV modulation, the normalized sampling frequency f_{sn} should be an integer multiple of ie, $T \geq 6nT_s$ for n = 1,2,3......... Hence all the six sectors will be equally used in one period for producing symmetric line output voltages


$v_{c\alpha}$
$v_{c\beta}$
ωt
90
180
270
360
Modulating signals
S_1
on
ωt
0
90
180
270
360
Switch S_1 state
S_3
on
ωt
0
90
180
270
360
Switch S_3 state
v_{ab}
v_{ab1}
v_i
ωt
0
90
180
270
360

Switching Segments for all SVM Sectors

Sector	Segment	1	2	3	4	5	6	7
1	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_1$	$\mathbf{V}_2$	$\mathbf{V}_7$	$\mathbf{V}_2$	$\mathbf{V}_1$	$\mathbf{V}_0$
	State	000	100	110	111	110	100	000
2	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_3$	$\mathbf{V}_2$	$\mathbf{V}_7$	$\mathbf{V}_2$	$\mathbf{V}_3$	$\mathbf{V}_0$
	State	000	010	110	111	110	010	000
3	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_3$	$\mathbf{V}_4$	$\mathbf{V}_7$	$\mathbf{V}_4$	$\mathbf{V}_3$	$\mathbf{V}_0$
	State	000	010	011	111	011	010	000
4	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_5$	$\mathbf{V}_4$	$\mathbf{V}_7$	$\mathbf{V}_4$	$\mathbf{V}_5$	$\mathbf{V}_0$
	State	000	001	011	111	011	001	000
5	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_5$	$\mathbf{V}_6$	$\mathbf{V}_7$	$\mathbf{V}_6$	$\mathbf{V}_5$	$\mathbf{V}_0$
	State	000	001	101	111	101	001	000
6	**Vector**	$\mathbf{V}_0$	$\mathbf{V}_1$	$\mathbf{V}_6$	$\mathbf{V}_7$	$\mathbf{V}_6$	$\mathbf{V}_1$	$\mathbf{V}_0$
	State	000	100	101	111	101	100	000

Over-modulation

- In over-modulation, the reference vector follows a circular trajectory that extends the bounds of the hexagon
- The portions of the circle inside the hexagon utilize the same SVM equations for determining the state times T_n, $T_{n+}1$ and T_z such that

$$T_1 = T_s M \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_2 = T_s M \sin(\theta)$$

$$T_z = T_s - T_1 - T_2$$

Over-modulation

- The portions of the circle outside the hexagon are limited by the boundaries of the hexagon and the corresponding time states T_n and T_{n+1} can be obtained as

$$T_n = T_s \frac{\sqrt{3}\cos(\theta) - \sin(\theta)}{\sqrt{3}\cos(\theta) + \sin(\theta)}$$

$$T_{n+1} = T_s \frac{2\sin(\theta)}{\sqrt{3}\cos(\theta) + \sin(\theta)}$$

$$T_z = T_s - T_1 - T_2 = 0$$

- Maximum modulation index M for SVM is $M_{max} = 2/\sqrt{3}$
- For $0 < M < 1$, the inverter operates in the normal SVM
- For $M > 2/\sqrt{3}$, the inverter operates completely in the six-step output mode
- Six-step operation switches the inverter only to the six vectors as shown in table, thereby minimizing the number of switching at one time

Switch States for Three-Phase Voltage-Source Inverter

State	State No.	Switch States	v_{ab}	v_{bc}	v_{ca}	Space Vector
S_1, S_2, and S_6 are on and S_4, S_5, and S_3 are off	1	100	V_S	0	$-V_S$	$\mathbf{V}_1 = 1 + j0.577 = 2/\sqrt{3}\angle 30°$
S_2, S_3, and S_1 are on and S_5, S_6, and S_4 are off	2	110	0	V_S	$-V_S$	$\mathbf{V}_2 = j1.155 = 2/\sqrt{3}\angle 90°$
S_3, S_4, and S_2 are on and S_6, S_1, and S_5 are off	3	010	$-V_S$	V_S	0	$\mathbf{V}_3 = -1 + j0.577 = 2/\sqrt{3}\angle 150°$
S_4, S_5, and S_3 are on and S_1, S_2, and S_6 are off	4	011	$-V_S$	0	V_S	$\mathbf{V}_4 = -1 - j0.577 = 2/\sqrt{3}\angle 210°$
S_5, S_6, and S_4 are on and S_2, S_3, and S_1 are off	5	001	0	$-V_S$	V_S	$\mathbf{V}_5 = -j1.155 = 2/\sqrt{3}\angle 270°$
S_6, S_1, and S_5 are on and S_3, S_4, and S_2 are off	6	101	V_S	$-V_S$	0	$\mathbf{V}_6 = 1 - j0.577 = 2/\sqrt{3}\angle 330°$
S_1, S_3, and S_5 are on and S_4, S_6, and S_2 are off	7	111	0	0	0	$\mathbf{V}_7 = 0$
S_4, S_6, and S_2 are on and S_1, S_3, and S_5 are off	8	000	0	0	0	$\mathbf{V}_0 = 0$

Over-modulation

- For $1 < M < 2/\sqrt{3}$, the inverter operates in over-modulation, which is normally used as a transitioning step from the SVM techniques into a six-step operation
- Over-modulation allows more utilization of the DC input voltage than the standard SVM techniques
  - But it results in non-sinusoidal output voltages with a high degree of distortion, especially at a low-output frequency

SVM Implementation

Steps

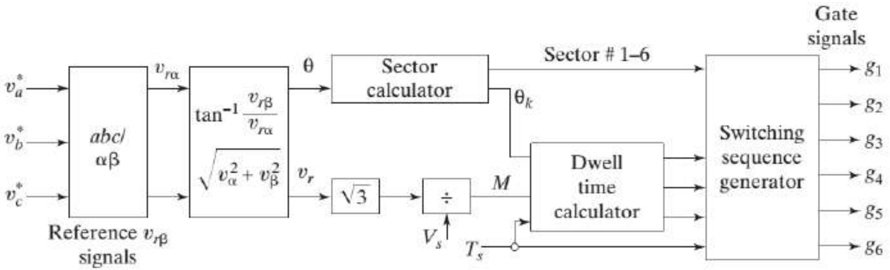
- Transformation from the three-phase reference signals to two-phase signals by abc to $\alpha - \beta$ transformation into two components $v_{r\alpha}$ and $v_{r\beta}$
- Find magnitude V_r and the angle θ of the reference vector

$$V_r = \sqrt{v_{r\alpha}^2 + v_{r\beta}^2}$$

$$\theta = \tan^{-1} \frac{v_{r\beta}}{v_{r\alpha}}$$

- Calculate the sector angle θ_k
- Calculate the modulation index M
- Calculate the dwell times T_1, T_2 and T_z
- Determine the gating signals and their sequence

Block Diagram



4. Comparison of Sine PWM & Space Vector PWM

- Any modulation scheme can be used to create the variable-frequency, variable-voltage ac waveforms
- **Sinusoidal PWM**
  - Sinusoidal PWM compares a high frequency triangular carrier with three sinusoidal reference signals (modulating signals), to generate the gating signals for the inverter switches
  - **Analog domain technique**
  - Commonly used in power conversion with both analog and digital implement
- Third-harmonic PWM
  - Cancellation of the third-harmonic components and better utilization of the DC supply
  - Preferred in three-phase applications

- **SV Method**
  - Does not consider each of the three modulating voltages as a separate identity
  - Three voltages are simultaneously taken into account within a two-dimensional reference frame ($\alpha - \beta$ plane) and the complex reference vector is processed as a single unit
  - Lower harmonics
  - Higher modulation index
  - Complete digital implementation by a single-chip microprocessor
  - Due to it's flexibility of manipulation, SVM is preferred in power converters and motor control

Summary of modulation schemes for Three-phase inverters with M = 1

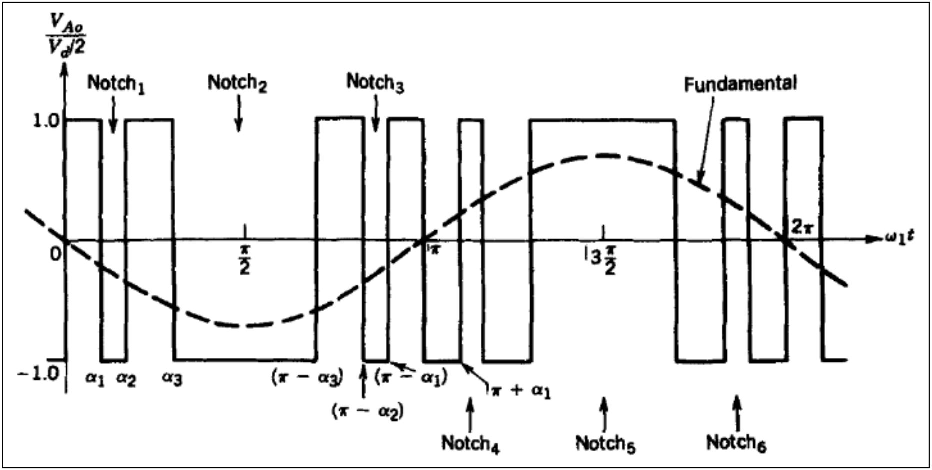
Summary of Modulation Techniques

Modulation Type	Normalized Phase Voltage, V_p/V_S	Normalized Line Voltage, V_L/V_S	Output Waveform
Sinusoidal PWM	0.5	$0.5 \times \sqrt{3} = 0.8666$	Sinusoidal
60° PWM	$1/\sqrt{3} = 0.57735$	1	Sinusoidal
Third-harmonic PWM	$1/\sqrt{3} = 0.57735$	1	Sinusoidal
SVM	$1/\sqrt{3} = 0.57735$	1	Sinusoidal
Overmodulation	Higher than the value for $M = 1$	Higher than the value for $M = 1$	Nonsinusoidal
Six-step	$\sqrt{2}/3 = 0.4714$	$\sqrt{(2/3)} = 0.81645$	Nonsinusoidal

5. Programmed Harmonic Elimination Switching

- **Selective Harmonic Elimination Switching**
- Combines square-wave switching and PWM
  - To control fundamental output voltage
  - To eliminate the designated harmonics from the output

5. Programmed Harmonic Elimination Switching



5. Programmed Harmonic Elimination Switching

- V_{Ao} of an inverter leg, normalized by $1/2V_d$ is plotted
- Six notches are introduced in the otherwise square-wave output, to control the magnitude of the fundamental voltage and to eliminate fifth and seventh harmonics
- On a half-cycle basis, each notch provides one degree of freedom
  - Having three notches per half-cycle provides control of fundamental and elimination of two harmonics (in this case fifth and seventh)
- Output waveform has odd half-wave symmetry $\implies$ only odd harmonics (coefficients of sine series) will be present
- In three-phase inverter, third harmonic and its multiples are cancelled out in the output
  - These harmonics need not be eliminated from the output of the inverter leg by means of waveform notching
- Switching frequency of a switch is seven times the switching frequency associated with a square-wave operation

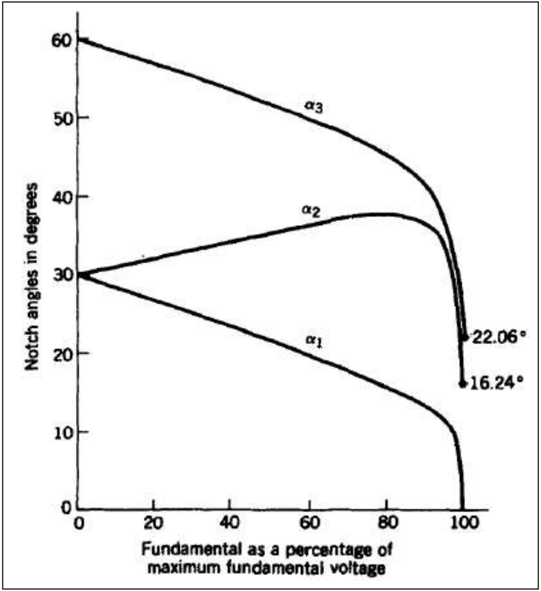
- In a square-wave operation, the fundamental-frequency voltage component

$$\frac{(\hat{V}_{Ao})_1}{V_d/2} = \frac{4}{\pi} = 1.273$$

- Maximum available fundamental amplitude is reduced because of the notches to eliminate fifth and seventh harmonics

$$\frac{(\hat{V}_{Ao})_{1,\max}}{V_d/2} = 1.188$$

- The required values of α_1, α_2 and α_3 are plotted as a function of the normalized fundamental in the output voltage

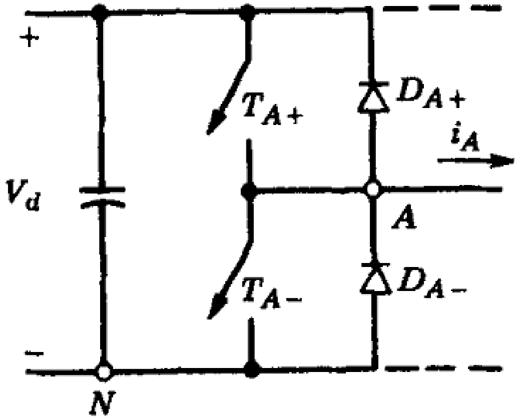

60
50
40
30
20
10
0
Notch angles in degrees
α_3
α_2
α_1
22.06°
16.24°
0
20
40
60
80
100
Fundamental as a percentage of maximum fundamental voltage

5. Programmed Harmonic Elimination Switching

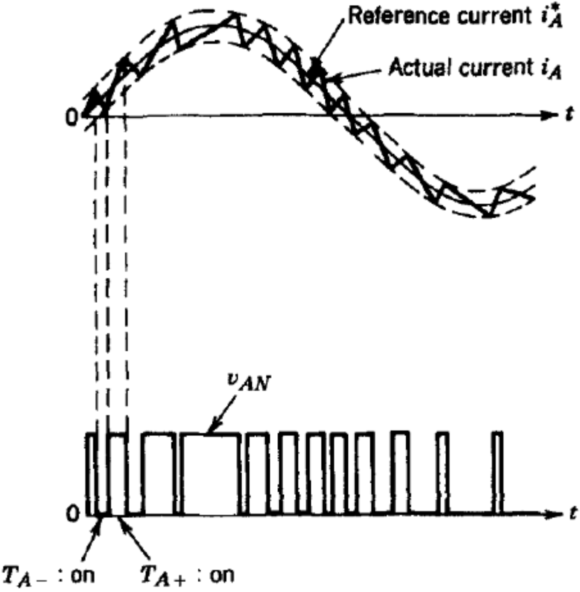
- To allow control over the fundamental output and to eliminate the 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics, five notches per half-cycle would be needed
  - Each switch would have 11 times the switching frequency compared with a square-wave operation
- Programmed harmonic elimination scheme can be implemented with the help of very large scale integrated (VLSI) circuits and microcontrollers
- Without making the switching frequency (and therefore the switching losses) very high, it allows the undesirable lower order harmonics to be eliminated
- Higher order harmonics can be filtered by a small filter, if necessary
- Before selecting this technique, it should be compared with a sinusoidal PWM technique with a low m_f to evaluate which one is better
- Distortions due to the blanking time, will occur

6. Current Controlled Voltage Source Inverter

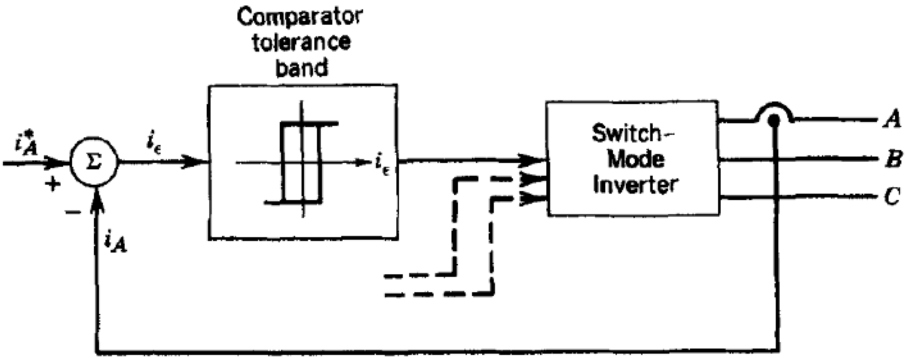
- Motor servo drives $\rightarrow$ Motor current (supplied by the switch-mode converter or inverter) needs to be controlled
- Output-stage current can be controlled in order to regulate the output voltage
- Control schemes are used to generated switching signals for the inverter switches in order to control the inverter output current
    1. Tolerance Band Control
    2. Fixed-Frequency Control


+
V_d
−
N
T_{A+}
T_{A-}
D_{A+}
D_{A-}
i_A
A

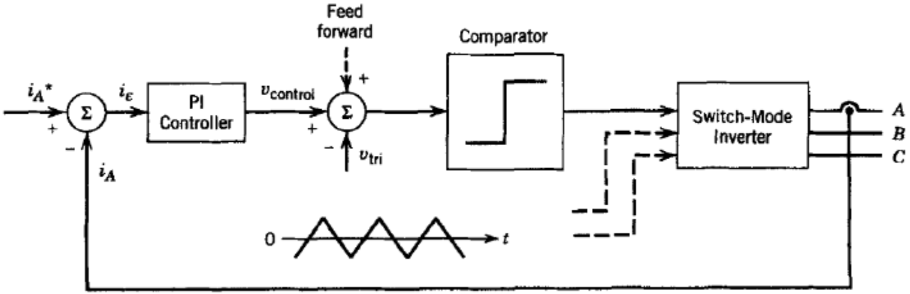
6.1 Tolerance Band Control



6.1 Tolerance Band Control



- **Hysteresis Current Control**
- Sinusoidal reference current: i_{A*}
- Actual phase current: i_A
- Actual phase current is compared with the tolerance band around the reference current associated with that phase
- If the actual current tries to go beyond the upper tolerance band, T_{A-} is turned ON $\implies$ T_{A+} is turned OFF
- The opposite switching occurs if the actual current tries to go below the lower tolerance band
- Switching frequency depends on how fast the current changes from the upper limit to the lower limit and vice versa $\rightarrow$ it depends on V_d, load back-emf, and the load inductance
- Switching frequency **does not remain constant** but varies along the current waveform



Feed forward
Comparator
i_A^*
i_ε
PI Controller
$v_{control}$
Σ
Switch-Mode Inverter
A
B
C
i_A
v_{tri}
0
t

- Error between the reference and the actual current is amplified or fed through a proportional integral (PI) controller
- Output $v_{control}$ of the amplifier is compared with a fixed-frequency (switching frequency f_s) triangular waveform v_{tri}
- A positive error $(i_{A*} - i_A) \rightarrow$ a positive $v_{control} \rightarrow$ results in a larger inverter output voltage $\rightarrow$ brings i_A back to it's reference value
- The load voltage (derived from the model of the load) is used as a compensating feed forward signal

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2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

*for private circulation only

Switched Mode Power Converters

(S6 EEE - EE364)

Prof. Dinto Mathew
Asst. Professor

Dept. of EEE, MACE

Overview I

Overview II

- M Type
- ZVS Resonant Converter
- Comparison of ZCS & ZVS Resonant Converters

1. Resonant Converters

- Switch-mode converters
  - Required to turn ON and turn OFF the entire load current during each switching switch-mode operation
    - Switches are subjected to high switching stresses
    - High switching power loss
    - Switching power loss increases linearly with the switching frequency of the PWM
    - EMI produced due to large di/dt and dv/dt caused by switch-mode operation

1. Resonant Converters

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- Higher switching frequency
  - Reduces converter size and weight
  - Increases power density

1. Resonant Converters

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    - High switching power loss
    - Switching power loss increases linearly with the switching frequency of the PWM
    - EMI produced due to large di/dt and dv/dt caused by switch-mode operation
- Higher switching frequency
  - Reduces converter size and weight
  - Increases power density
- To realize high switching frequencies in converters
  - Switch in a converter should change its status (from ON to OFF or vice versa) when the voltage across it and/or the current through it is zero at the switching instant $\Longrightarrow$ **Zero-voltage Switching** and/or **Zero-current Switching** $\rightarrow$ **Resonant Converters**

- Converter topologies & switching strategies that result in zero-voltage and/or zero-current switchings

- Converter topologies & switching strategies that result in zero-voltage and/or zero-current switchings

Classification

1. Load-resonant Converters
2. Resonant-switch Converters
3. Resonant-DC-link Converters
4. High-frequency-link integral-half-cycle Converters

Load Resonant Converters

- LC resonant tank circuit is used
- Oscillating v & i, due to LC resonance in the tank are applied to the load, and the converter switches can be switched at zero voltage and/or zero current instant
- Series LC or Parallel LC circuit
- Power flow to the load is controlled by the resonant tank impedance, which in turn is controlled by the switching frequency f_s, in comparison to the resonant frequency f_o, of the tank

Load Resonant Converters

- LC resonant tank circuit is used
- Oscillating v & i, due to LC resonance in the tank are applied to the load, and the converter switches can be switched at zero voltage and/or zero current instant
- Series LC or Parallel LC circuit
- Power flow to the load is controlled by the resonant tank impedance, which in turn is controlled by the switching frequency f_s, in comparison to the resonant frequency f_o, of the tank

Classification

1. Voltage-source Series-resonant Converters
   a. Series-loaded Resonant (SLR) Converters
   b. Parallel-loaded Resonant (PLR) Converters
   c. Hybrid-resonant Converters
2. Current-source Parallel-resonant Converters
3. Class E and Subclass E Resonant Converters

- **Quasi-resonant converters**
- During one switching-frequency time period, there are resonant as well as non-resonant operating intervals

Resonant Switch Converters

- **Quasi-resonant converters**
- During one switching-frequency time period, there are resonant as well as non-resonant operating intervals

Classification

1. Resonant-switch dc-dc converters
   1. Zero-current-switching (ZCS) converters
   2. Zero-voltage-switching (ZVS) converters
2. Pseudo-resonant converter and Clamped-voltage converter (Resonant-transition converter)

Resonant DC Link Converters

- Conventional switch-mode PWM DC-AC inverters
  - Input V_d is a fixed-magnitude DC
  - Sinusoidal output is obtained by switch-mode PWM switchings

- Conventional switch-mode PWM DC-AC inverters
  - Input V_d is a fixed-magnitude DC
  - Sinusoidal output is obtained by switch-mode PWM switchings

Resonant DC Link Converters

- Input voltage is made to oscillate around V_d, by means of an LC resonance so that the input voltage remains zero for a finite duration during which the status of the inverter switches can be changed $\Longrightarrow$ **Zero-voltage switching**

High-frequency-link integral-half-cycle Converters

- Input is a high-frequency sinusoidal AC supply
- Bidirectional switches are used
- Low-frequency AC output of adjustable magnitude and frequency OR an adjustable-magnitude DC
- Switches are turned ON and OFF at the zero crossings of the input voltage

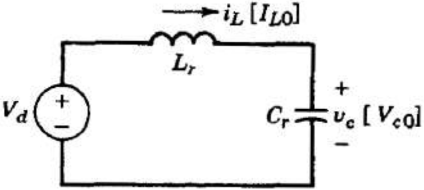
2. Basic Resonant Circuit Concepts

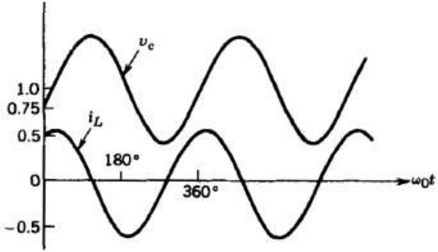
- Generalized analysis of resonant converters
- Initial conditions are indicated by uppercase letters, Subscript 0, and square brackets $\rightarrow [V_{c0}]$ and $[I_{L0}]$

3. Series Resonant Circuit

Analysis of Series Resonant Circuit :

1. Undamped Series-Resonant Circuit
2. Series-Resonant Circuit with Capacitor-Parallel Load
3. Frequency Characteristics of Series-Resonant Circuit





$I_{L0} = 0.5,\ V_{c0} = 0.75$

- State variables
  - Inductor current i_L
  - Capacitor voltage v_c

$$L_r \frac{di_L}{dt} + v_c = V_d$$

$$C_r \frac{dv_c}{dt} = i_L$$

$$i_L(t) = I_{L0} \cos \omega_0 (t - t_0) + \frac{V_d - V_{c0}}{Z_o} \sin \omega_0 (t - t_0)$$

$$v_c(t) = V_d - (V_d - V_{c0}) \cos \omega_0 (t - t_0) + Z_0 I_{L0} \sin \omega_0 (t - t_0)$$

- Angular resonance frequency

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}}$$

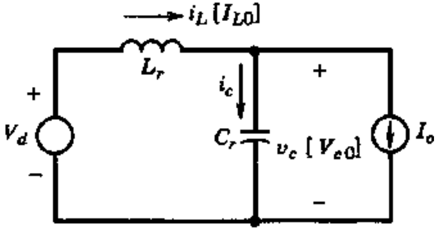
- Characteristic impedance

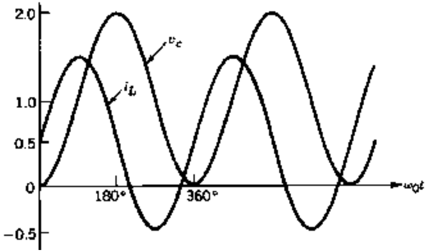
3.1 Undamped Series-Resonant Circuit III

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \quad \Omega$$

$$V_{\text{base}} = V_d$$

$$I_{\text{base}} = \frac{V_d}{Z_0}$$





- Capacitor is in parallel with a current source I_o, which represents the load
- DC quantities : V_d and I_o
- Initial conditions at t_o : I_{Lo} and V_{co}

$$v_c = V_d - L_r \frac{di_L}{dt}$$

$$i_L - i_c = I_o$$

$$i_c = C_r \frac{dv_c}{dt} = -L_r C_r \frac{d^2 i_L}{dt^2}$$

$$\frac{d^2 i_L}{dt^2} + \omega_0^2 i_L = \omega_0^2 I_o$$

where ω_0 is the angular frequency

$$i_L(t) = I_o + (I_{L0} - I_o)\cos\omega_0(t - t_0) + \frac{V_d - V_{c0}}{Z_0}\sin\omega_0(t - t_0)$$

$$v_c(t) = V_d - (V_d - V_{c0})\cos\omega_0(t - t_0) + Z_0(I_{L0} - I_o)\sin\omega_0(t - t_0)$$

where Z_0 is the characteristic impedance

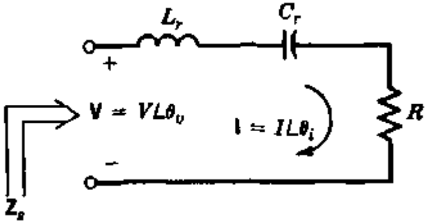
- If $V_{c0} = 0$ and $I_{L0} = I_0$ then

$$i_L(t) = I_o + \frac{V_d}{Z_0} \sin \omega_0 (t - t_0)$$

and

$$v_c(t) = V_d [1 - \cos \omega_0 (t - t_0)]$$

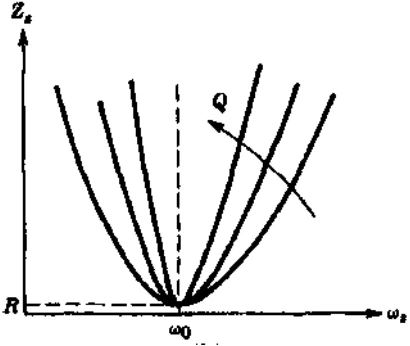
- Resonance frequency: ω_0
- Characteristic impedance: Z_0



- **Quality Factor (Q)**

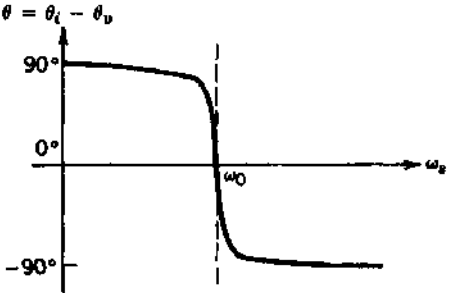
$$Q = \frac{\omega_0 L_r}{R} = \frac{1}{\omega_0 C_r R} = \frac{Z_0}{R}$$

3.3 Frequency Characteristics of Series-Resonant Circuit II

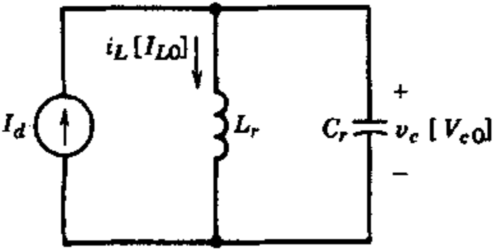


- Magnitude Z_s of the circuit impedance as a function of frequency with Q as a parameter, keeping R constant
- Z_s is a pure resistance equal to R at $\omega_s = \omega_0$ and is very sensitive to frequency deviation from ω_0 at higher values of Q

3.3 Frequency Characteristics of Series-Resonant Circuit III



- Current phase angle $\theta(= \theta_i - \theta_v)$ as a function of frequency
- At frequencies below $\omega_0(\omega_s < \omega_0)$
    - Current leads voltage
    - Capacitor impedance dominates over inductor impedance
- At frequencies above $\omega_0(\omega_s > \omega_0)$
    - Current lags voltage
    - Inductor impedance dominates over the capacitor impedance



- Undamped parallel-resonant circuit supplied by a dc current I_d
- Initial conditions at time $t = t_0$: I_{L0} and V_{c0}
- State variables
  - Inductor current i_L
  - Capacitor voltage V_c

4.1 Undamped Parallel Resonant Circuit II

$$i_L + C_r \frac{dv_c}{dt} = I_d$$

$$v_c = L_r \frac{di_L}{dt}$$

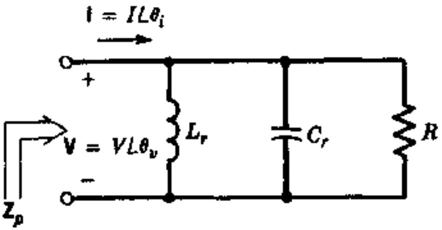
- Solution for $t \geq t_0$

$$i_L(t) = I_d + (I_{L0} - I_d)\cos \omega_0(t - t_0) + \frac{V_{c0}}{Z_0}\sin \omega_0(t - t_0)$$

$$v_c(t) = Z_0(I_d - I_{L0})\sin \omega_0(t - t_0) + V_{c0}\cos \omega_0(t - t_0)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \qquad Z_0 = \sqrt{\frac{L_r}{C_r}}$$

4.2 Frequency Characteristics of Parallel-Resonant Circuit I



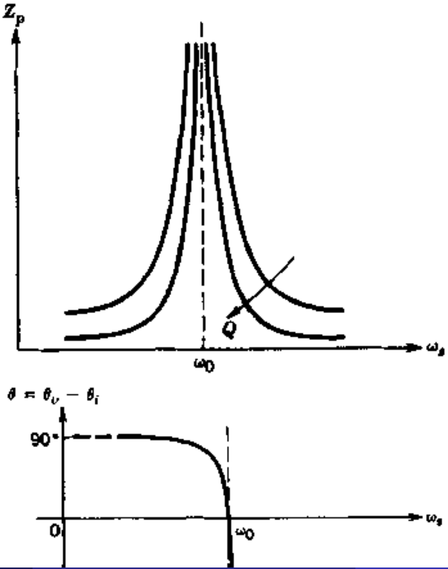
- Resonance frequency: ω_0
- Characteristic Impedance: Z_0
- With Load Resistor R $\rightarrow$ **Quality Factor(Q)**

4.2 Frequency Characteristics of Parallel-Resonant Circuit II

$$Q = \omega_0 R C_r = \frac{R}{\omega_0 L_r} = \frac{R}{Z_0}$$

- **Characteristics**

4.2 Frequency Characteristics of Parallel-Resonant Circuit III



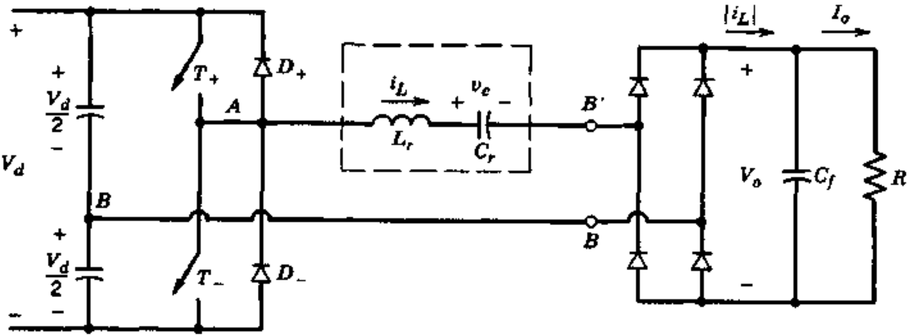
4.2 Frequency Characteristics of Parallel-Resonant Circuit IV

- Magnitude Z_p, of the circuit impedance as a function of frequency with Q as a parameter, keeping R constant
- Voltage phase angle $\theta(=\theta_v - \theta_i)$ as a function of frequency
  - For frequencies below $\omega_0(\omega_s < \omega_0)$, voltage leads the current $\rightarrow$ Inductor impedance is lower than the capacitor impedance $\rightarrow$ Inductor current dominates
  - For frequencies above $\omega_0(\omega_s > \omega_0)$, capacitor impedance is lower $\rightarrow$ Voltage lags the current with the voltage phase angle θ approaching -90^0

5. Load Resonant Converter

- LC tank is used
  - Oscillating load voltage and current
  - Provides zero-voltage and/or zero-current switchings
- Only the steady-state operation is considered in the analysis

- Half-bridge configuration of the SLR converter



- Transformer can be used
  - To provide the output voltage of a desired magnitude

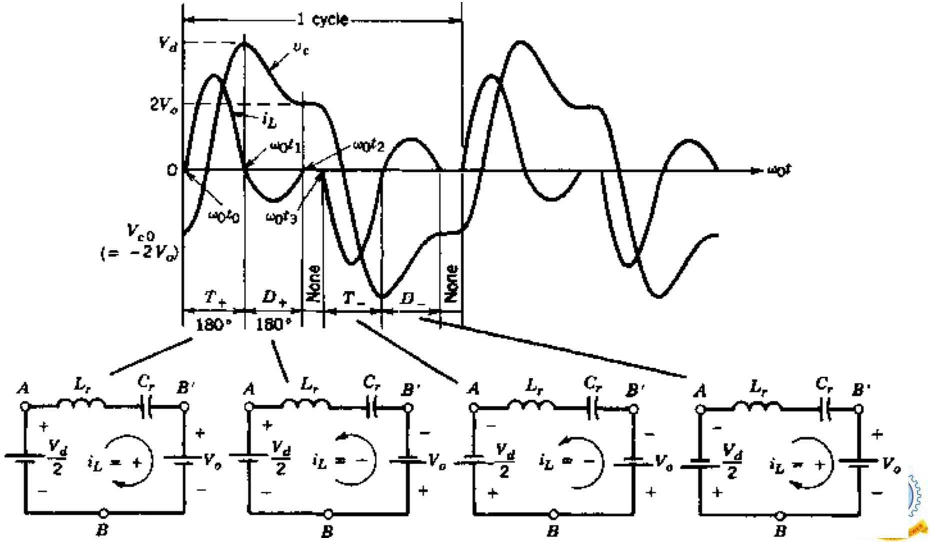
- To provide electrical isolation between the input and the output
- Series-resonant Tank Circuit
  - Output load appears in series with the resonant tank
  - L_r and C_r
  - Current through the resonant tank circuit is full-wave rectified at the output
  - $|i_L|$ feeds the output stage
- Filter capacitor C $\implies$ Output voltage across the capacitor can be assumed to be a DC voltage without any ripple
- Resistive power loss in the resonant circuit is assumed to be negligible
- Output voltage V_0, is reflected across the rectifier input as $V_{B'B}$
  - $V_{B'B} = V_0$, if i_L is positive
    - i_L flows through T_+, if it is ON, otherwise it flows through the diode D_-
  - $V_{B'B} = -V_0$, if i_L is negative

    - i_L flows through T_-, if it is ON, otherwise it flows through the diode D_+

- For $i > 0$
  - T_+ conducting
    - $v_{AB} = +\frac{1}{2}V_d$ and $v_{AB'} = +\frac{1}{2}V_d - V_o$
  - D_- conducting
    - $v_{AB} = -\frac{1}{2}V_d$ and $v_{AB'} = -\frac{1}{2}V_d - V_o$
- For $i < 0$
  - T_- conducting
    - $v_{AB} = -\frac{1}{2}V_d$ and $v_{AB'} = -\frac{1}{2}V_d + V_o$
  - D_+ conducting
    - $v_{AB} = +\frac{1}{2}V_d$ and $v_{AB'} = +\frac{1}{2}V_d + V_o$
- Voltage applied across the tank $(v_{AB'})$ depends on
  - Which device is conducting
  - Direction of i_L

5.1 Series Loaded Resonant DC-DC Converters IV

- In steady-state symmetrical operation, both the switches are operated identically
- In SLR converter, output voltage (V_0), cannot exceed the input voltage $(+\frac{1}{2}V_d\ ) \implies V_0 < +\frac{1}{2}V_d$
- Switching frequency $f_s(=\omega_s/2\pi)$ can be controlled to be less than or greater than the resonance frequency $f_0(=\omega_0/2\pi)$ if the converter consists of self-controlled switches
- Three possible modes of operation based on the ratio of switching frequency ω_s, to the resonance frequency ω_0, which determines if i_L flows continuously or discontinuously


1 cycle
V_d
v_c
$2V_o$
i_L
$\omega_0 t_1$
$\omega_0 t_2$
0
$\omega_0 t$
$\omega_0 t_0$
$\omega_0 t_3$
V_{c0}
$(= -2V_o)$
None
None
T_+
D_+
T_-
D_-
180°
180°
A
L_r
C_r
B'
$\frac{V_d}{2}$
i_L
V_o
B

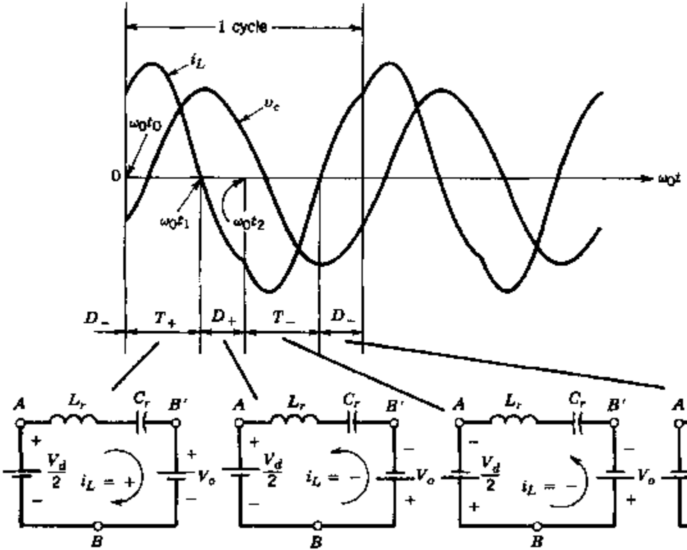
Discontinuous-Conduction Mode with $(\omega_s < \frac{1}{2}\omega_0)$ II

- Waveforms in steady state condition are analyzed
- At $\omega_0 t_o$, switch T_+, is turned ON
  - i_L builds up from it's zero value
  - Capacitor voltage builds up from it's initial negative value $V_{co} = -2V_o$
- After 180^o subsequent to $\omega_0 t_o$, at $\omega_0 t_1$
  - Inductor current reverses $\rightarrow$ flows through D_+, since T_- is not yet turned ON
- After 180^o subsequent to $\omega_0 t_1$, at $\omega_0 t_2$
  - i_L goes to zero and remains zero as no switches are ON
- Symmetrical operation requires that v_c, during the discontinuous interval $\omega_0(t_3 - t_2)$ be negative of $V_{co} \implies 2V_o$
- At $\omega_0 t_3$
  - T_- is turned ON
  - Next half-cycle ensues

Discontinuous-Conduction Mode with ($\omega_s < \frac{1}{2}\omega_0$) III

- Because of the discontinuous interval, one half-cycle of the operating frequency exceeds 360^0 of the resonance frequency $f_0 \implies$ Mode of operation with $\omega_s < \frac{1}{2}\omega_0$
  - Switches turn OFF naturally at zero current and at zero voltage, since the inductor current goes through zero
  - Switches turn ON at zero current but not at zero voltage
- Average of the rectified inductor current $|i_L| = I_0$
- **Disadvantage**
  - Relatively large peak current in the circuit $\rightarrow$ higher conduction losses, compared with the continuous-conduction mode

Continuous-Conduction Mode with $(\frac{1}{2}\omega_0 < \omega_s < \omega_0)$ I



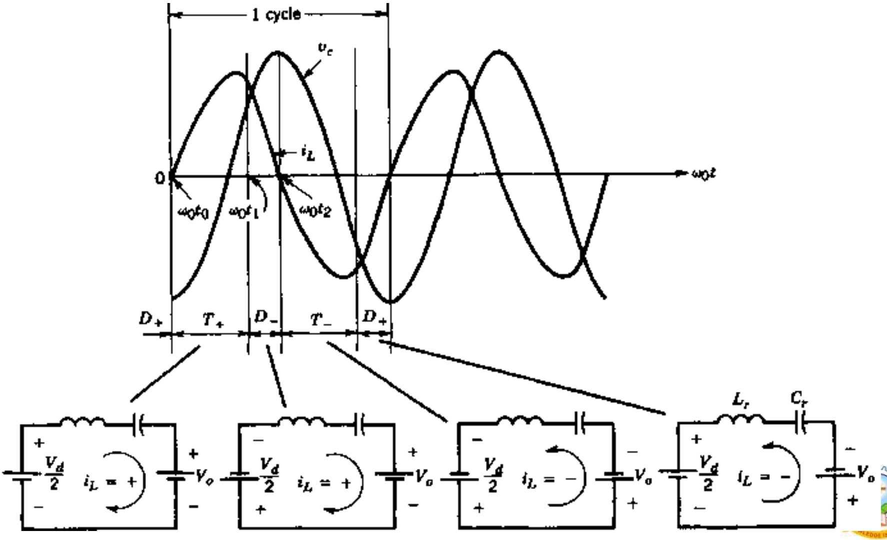
Continuous-Conduction Mode with ($\frac{1}{2}\omega_0 < \omega_s < \omega_0$) II

- Operation
  - At $\omega_0 t_0$
    - T_+ turns ON with a finite value of the inductor current and at a preconduction switch voltage of V_d
    - T^+ conducts for less than 180^0
  - At $\omega_0 t_1$
    - i_L reverses and flows through D_+
    - T_+ turns OFF naturally
  - At $\omega_0 t_2$
    - T_- is turned ON
    - i_L transfers from D_+ to T_-
- D_+, conducts for less than 180^o because T_- is switched ON early, compared with the discontinuous-conduction mode
- In this mode of operation, the switches turn ON at a finite current and at a finite voltage, thus resulting in a turn-on switching loss

Continuous-Conduction Mode with ($\frac{1}{2}\omega_0 < \omega_s < \omega_0$) III

- Freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse current spikes flowing through the switches
- Turn-off switches occurs naturally at zero current and at zero voltage as the inductor current through them goes to zero and reverses through the freewheeling diodes $\rightarrow$ Possible to use thyristors as switches in low switching-frequency applications

Continuous-Conduction Mode with ($\omega_s > \omega_0$) I



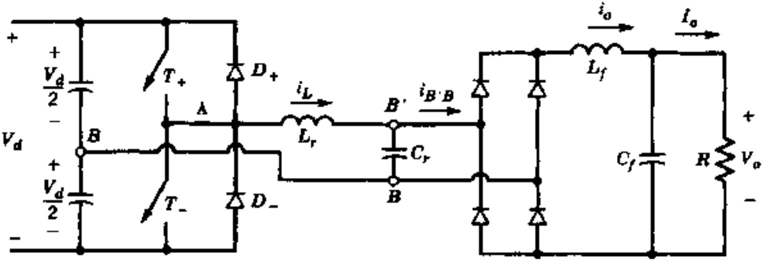
Continuous-Conduction Mode with ($\omega_s > \omega_0$) II

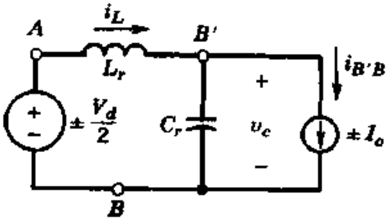
- Switches in this mode with $\omega_s > \omega_0$ are forced to turn OFF a finite current, but they are turned ON at zero current and zero voltage
- Operation
  - At $\omega_0 t_0$
    - T_+ starts conduction at zero current when the inductor current reverses in direction
  - At $\omega_0 t_1$
    - T_+ is forced to turn OFF before the half-cycle of the current oscillation ends
    - Positive i_L is forced to flow through D_-
  - At $\omega_0 t_2$
    - Current through the diode reaches zero quickly
    - T_- is gated on as soon as D_- begins to conduct so that it can conduct when i_L reverses
    - Combined conduction interval for T_+ and D_- is equal to one half-cycle of operation at the switching frequency of ω_s
      $\implies \omega_s > \omega_0$
- **Advantages**

Continuous-Conduction Mode with ($\omega_s > \omega_0$) III

- Switches turn ON at a zero current and zero voltage
- Freewheeling diodes do not need to have very fast reverse-recovery characteristics

- **Disadvantages**
  - Switches need to force turn OFF near the peak of i_L, thus causing a large turn-off switching loss


$+$
V_d
$+$
$\frac{V_d}{2}$
$-$
$+$
$\frac{V_d}{2}$
$-$
$-$
B
T_+
T_-
D_+
D_-
A
i_L
L_r
B'
$i_{B'B}$
C_r
B
i_o
I_o
L_f
C_f
R
$+$
V_o
$-$


A
i_L
L_r
B'
$i_{B'B}$
$\pm\frac{V_d}{2}$
C_r
$+$
v_c
$-$
$\pm I_o$
B

5.2 Parallel Loaded Resonant DC-DC Converters II

- Output stage is connected in parallel with the resonant-tank capacitor C_r
- Voltage across the resonant-tank capacitor C_r is rectified, filtered, and then supplied to the load
- Current through the output filter inductor can be assumed to be a ripple-free dc current I_o during a switching frequency time period based on an assumption of high switching frequency and a sufficiently large value of the filter inductor
- Voltage across the resonant tank depends on the devices conducting
  - T_+ or D_+ : **ON** $\implies v_{AB} = +\frac{1}{2}V_d$
  - T_- or D_- : **ON** $\implies v_{AB} = -\frac{1}{2}V_d$
- Input voltage to the tank (v_{AB})s equal in magnitude to $+\frac{1}{2}V_d$ but its polarity depends on which switch is turned on $(T_+, \text{or} T_-)$
- Current $i_{B'B}$ equals I_o in magnitude, but it's direction depends on the polarity of the voltage v_c across C_r

- **Parallel Loaded Resonant (PLR) Converter Vs Series Loaded Resonant (SLR) Converter**
  - PLR converters appear as a voltage source $\rightarrow$ Better suited for multiple outlets
  - PLR converters can step up as well as step down the voltage, unlike the SLR Converters, which can operate only as a step-down converter (not counting the transformer turns ratio)
  - Drawback of PLR converters is that it does not possess inherent short-circuit protection capability

- Shaping the switch voltage and switch current by LC resonant circuit $\rightarrow$ zero voltage and/or zero current switching $\rightarrow$ **Resonant Switch Converter**
- Types of **Resonant Switch Converters**
  1. **Zero Current Switching (ZCS)** Topology
     - Switch turns ON and OFF at zero current
     - Peak resonant current flows through the switch
     - Peak switch voltage remains the same as in its switch-mode counterpart

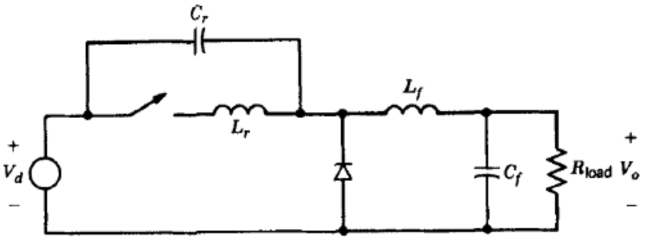


Figure : ZCS DC-DC Converter (Step-down)

2. **Zero Voltage Switching (ZVS)** Topology
   - Switch turns ON and OFF at zero voltage
   - Peak voltage appears across the switch
   - Peak switch current remains the same as in its switch-mode counterpart

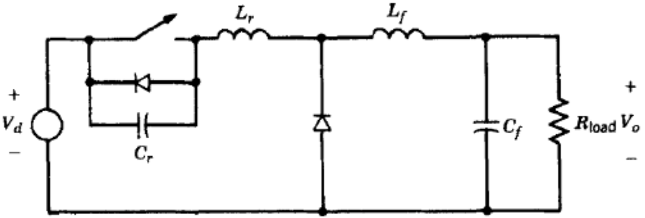


Figure : ZVS DC-DC Converter (Step-down)

3. **Zero Voltage Switching, Clamped Voltage (ZVS-CV)** Topology
   - Switch turns ON and OFF at zero voltage
   - Consists of at least one converter leg made up of two switches
   - Peak switch voltage remains the same as in its switch-mode counterpart
   - Peak switch current is higher

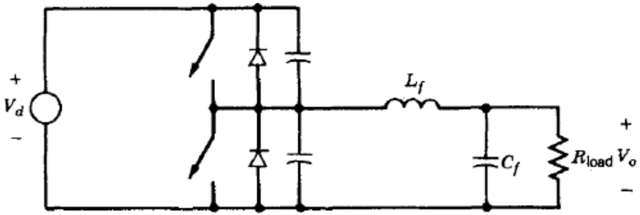
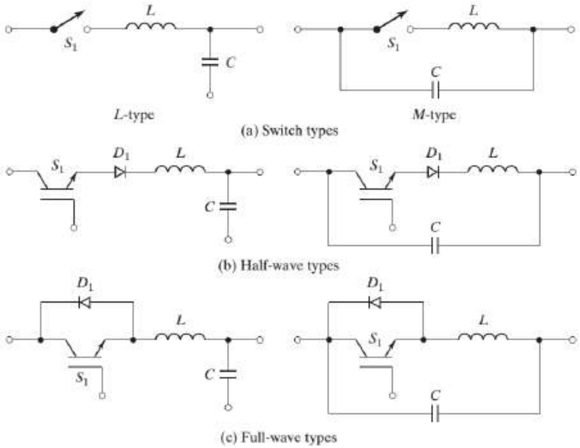


Figure : ZVS-CV DC-DC Converter (Step-down)

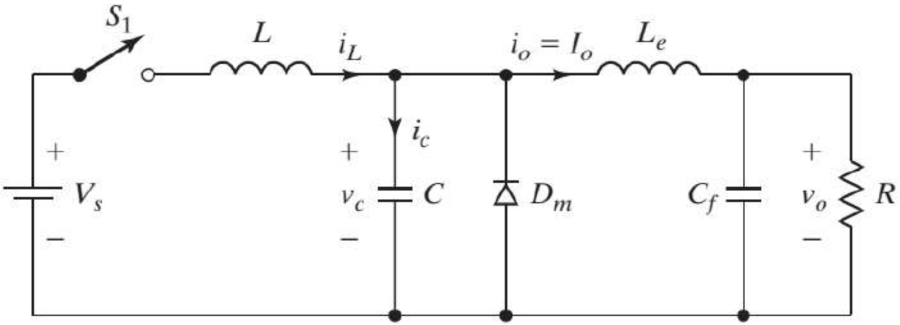
6.1 ZCS Resonant Converter I

- Switches turn ON and OFF at zero current
- Resonant circuit consists of switch S_1, inductor L, and capacitor C
- Inductor L is connected in series with a power switch S_1 to achieve ZCS
- Inductor L limits the di/dt of the switch current
- L and C constitute a series resonant circuit
- When switch current is zero, there is a current $i = C_f dv_T/dt$ flowing through the internal capacitance C_j due to a finite slope of the switch voltage at turn-off. This current flow causes power dissipation in the switch and limits the high switching frequency
- Switch Configurations
  - Half-wave configuration $\rightarrow$ diode D_1 allows unidirectional current flow
  - Full-wave configuration $\rightarrow$ switch current can flow bidirectionally

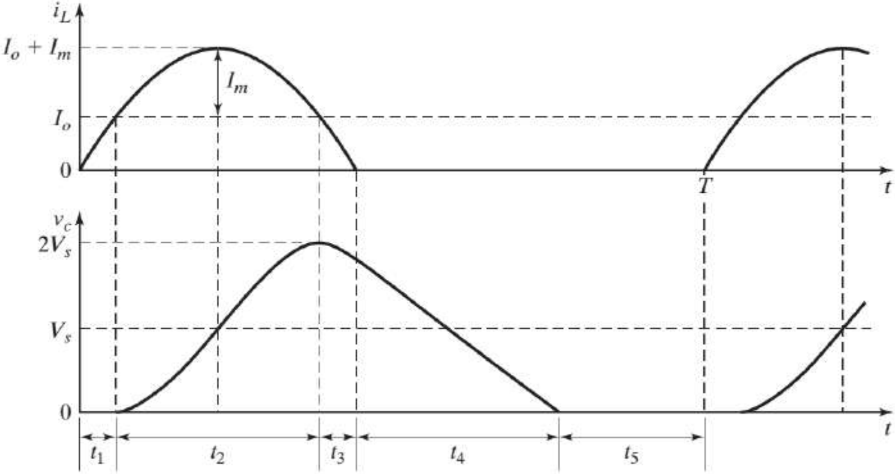
- For L-type configuration, C can be polarized electrolytic capacitance, whereas the capacitance C for the M-type configuration must be an ac capacitor



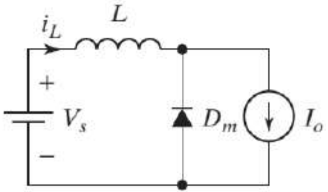
L Type I



L Type II



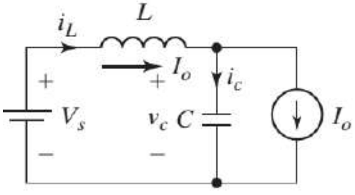
Mode 1



Mode 1

- Mode 1: $0 < t < t_1$
- Switch S_1 is turned ON
- Diode D_m conducts
- Inductor current i_L rises linearly $\rightarrow i_L = (V_s/L)t$
- Mode 1 ends at time $t = t_1$ when $i_L(t = t_1) = I_o \rightarrow t_1 = I_o L/V_s$

Mode 2



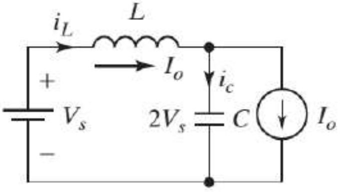
Mode 2

- Mode 2: $t_1 < t < t_2$
- Switch S_1 remains ON
- Diode D_m is OFF
- Inductor current $i_L = I_m \sin \omega_o t + I_o$
- $I_m = V_s \sqrt{C/L}$
- Capacitor voltage $v_c = V_s(1 - \cos \omega_o t)$

L Type V

- Peak switch current occurs at $t = (\pi/2)\sqrt{LC} \rightarrow I_p = I_m + I_o$,
- Peak capacitor voltage $V_{c(pk)} = 2V_s$
- Mode 2 ends at $t = t_2$ when $i_L(t = t_2) = I_o$ and $v_c(t = t_2) = V_{c2} 2V_s \;\rightarrow\; t_2 = \pi\sqrt{LC}$

Mode 3



Mode 3

- Mode 3: $t_2 < t < t_3$

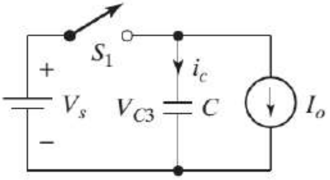
L Type VI

- Inductor current falls from I_o to zero

$$i_L = I_o - I_m \sin \omega_o t$$

- Capacitor voltage $v_c = 2V_s \cos \omega_o t$
- Mode 3 ends at $t = t_3$ when $i_L(t = t_3) = 0$ and $v_c = (t = t_3) = V_{c3} \ \rightarrow t_3 = \sqrt{LC} \sin^{-1}(1/x)$ where $x = I_m/I_o = (V_s/I_o)\sqrt{C/L}$

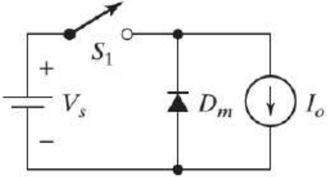
Mode 4



Mode 4

- Mode 4: $t_3 < t < t_4$
- Capacitor supplies the load current I_o
- $v_c = V_{c3} - (I_o/C)t$
- Mode 4 ends at time $t = t_4$ when $v_c(t = t_4) = 0 \;\rightarrow t_4 = V_{c3}C/I_o$

Mode 5



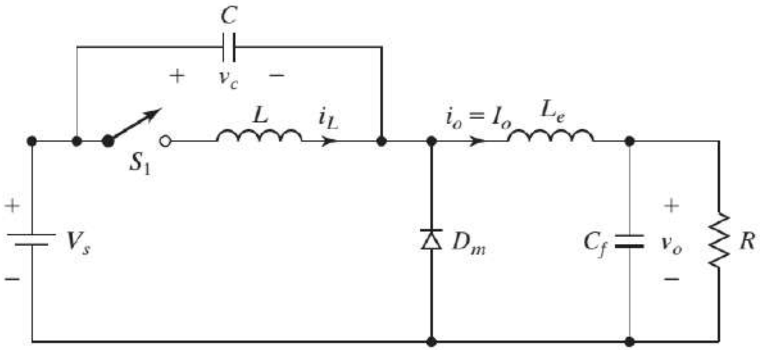
Mode 5

- Mode 5: $t_4 < t < t_5$
- Capacitor voltage tends to be negative

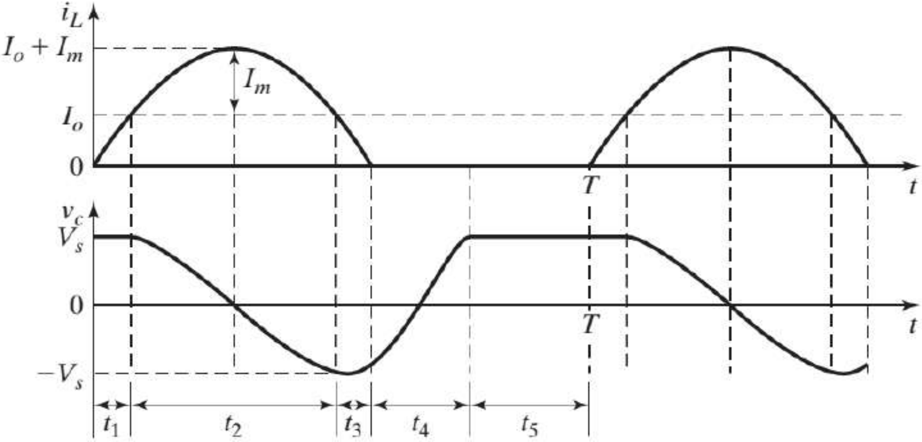
L Type VIII

- Diode D_m conducts
- Load current I_o flows through the diode D_m
- Mode 5 ends at $t = t_5$ when the switch S_1 is turned ON again
- $t_5 = T - (t_1 + t_2 + t_3 + t_4)$
- Peak switch voltage equals to the dc supply voltage V_s
- Since the switch current is zero at turn-on and turn-off, the switching loss becomes negligible
- By placing an antiparallel diode across the switch, the output voltage can be made insensitive to load variations

M Type I

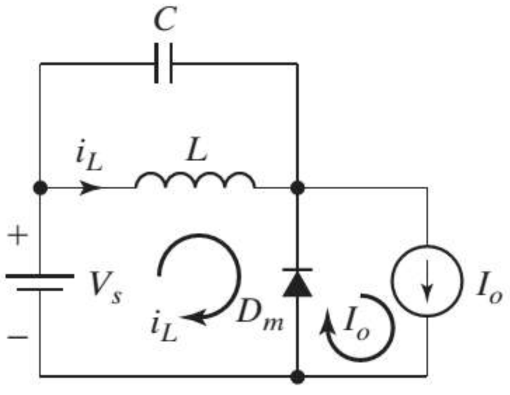


M Type II



- 5 Modes of operation

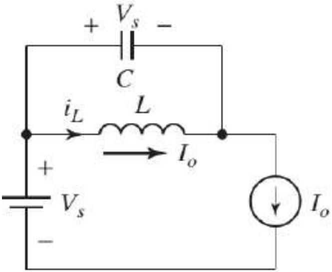
Mode 1



Mode 1

- Similar to L type

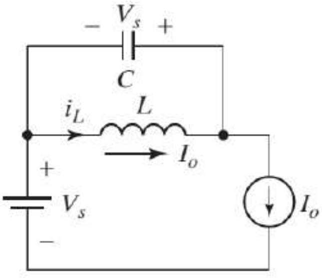
Mode 2



Mode 2

- Capacitor voltage $v_c = V_s \cos \omega_o t$
- Peak capacitor voltage, $V_c pk = V_s$
- Mode 2 ends at $t = t_2 \;\rightarrow v_c(t = t_2) = V_{c2} = -V_s$

Mode 3

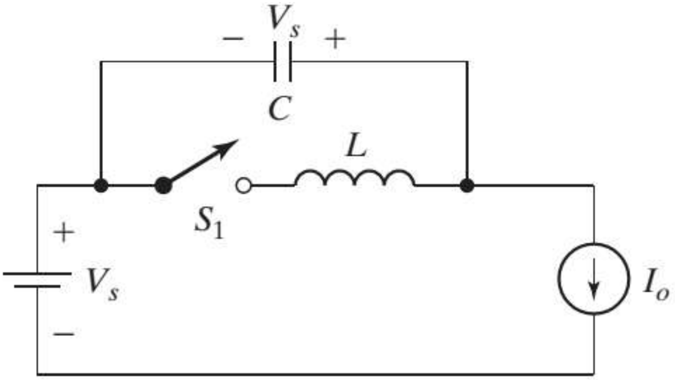


Mode 3

- Capacitor voltage $v_c = -V_s \cos \omega_o t$
- Mode 3 ends at $t = t_3 \rightarrow v_c(t = t_3) = V_{c3}$
- V_{c3} can have a negative value

M Type VI

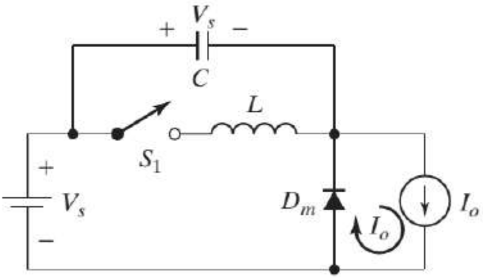
Mode 4



Mode 4

- Mode 4 ends at $t = t_4 \rightarrow v_c(t = t_4) = V_s \implies t_4 = (V_s - V_{c3})C/I_o$

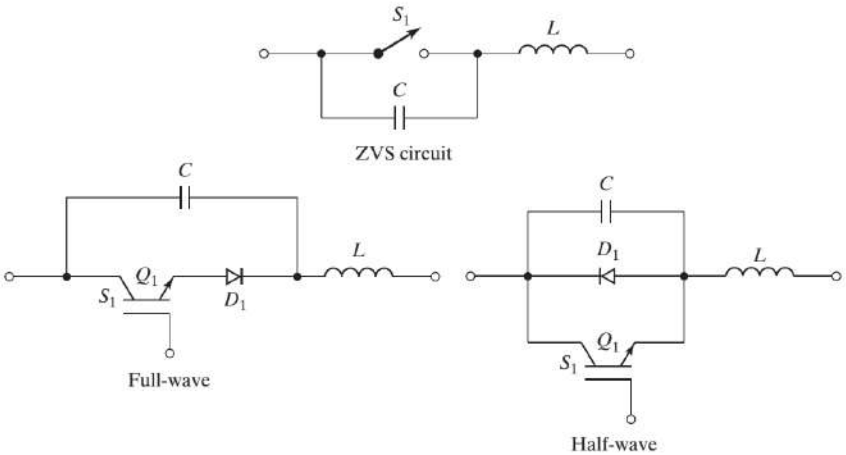
Mode 5



Mode 5

- Similar to L type

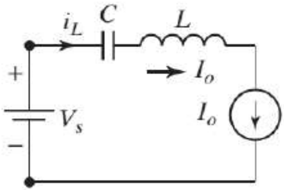
6.2 ZVS Resonant Converter I



- Capacitor C is connected in parallel with the switch S_1 to achieve ZVS

- Internal switch capacitance C_j is added with the capacitor C $\rightarrow$ it affects the resonant frequency
- **Half-wave configuration**: Switch is implemented with a transistor Q_1 and an antiparallel diode D_1 and the voltage across C is clamped by D_1
- **Full-wave configuration**: Diode D_1 is connected in series with Q_1 and the voltage across C can oscillate freely
- ZVS resonant converter is the dual of the ZCS resonant
- Equations for the M-type ZCS resonant converter can be applied if i_L is replaced by v_c and vice versa, L by C and vice versa and V_s by I_o and vice versa
- 5 modes of operation

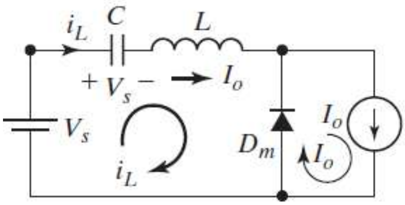
Mode 1



Mode 1

- Mode 1: $0 < t < t_1$
- Switch S_1 and diode D_m are OFF
- Capacitor C charges at a constant rate of load current I_o
- Capacitor voltage $v_c = (I_o/C)t$
- Mode 1 ends at time $t = t_1$ when $v_c(t = t_1) = V_s$ *ie* $t_1 = V_s C/I_o$

Mode 2

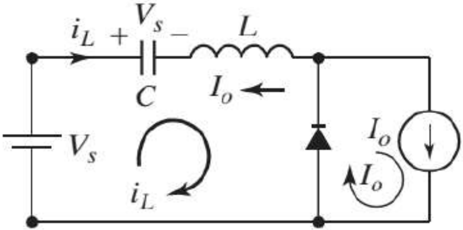


Mode 2

- Mode 2: $t_1 < t < t_2$
- S_1 is still OFF
- Diode D_m turns ON
- Capacitor voltage $v_c = V_m \sin \omega_o t + V_s$
- $V_m = I_o \sqrt{L/C}$

- Peak switch voltage, which occurs at $t = (\pi/2)\sqrt{LC}$ is given by $V_{T(pk)} = V_{c(pk)} = I_o\sqrt{L/C + V_s}$
- Inductor current $i_L = I_o \cos\omega_o t$
- Mode 2 ends at $t = t_2$ when $v_c(t = t_2) = V_s$ and $i_L(t = t_2) = -I_o \implies t_2 = \pi\sqrt{LC}$

Mode 3



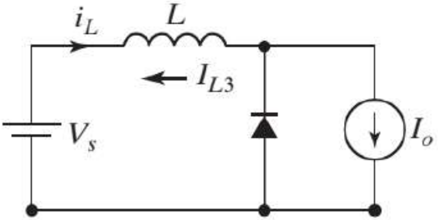
Mode 3

- Mode 3: $t_2 < t < t_3$
- Capacitor voltage falls from V_s to zero $\rightarrow v_c = V_s - V_m \sin \omega_o t$
- Inductor current $iL = -I_o \cos \omega_o t$

6.2 ZVS Resonant Converter VII

- Mode 3 ends at $t = t_3$ when $v_c(t = t_3) = 0$ and $i_L(t = t_3) = I_{L3} \;\rightarrow\; t_3 = \sqrt{LC}\sin^{-1} x$ where $x = V_s/V_m = (V_s/I_o)\sqrt{C/L}$

Mode 4



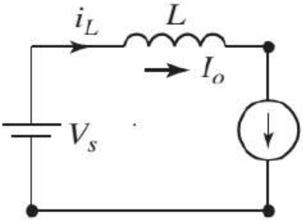
Mode 4

- Mode 4: $t_3 < t < t_4$
- Switch S1 is turned ON
- Diode D_m remains ON
- Inductor current rises linearly from I_{L3} to I_o $\rightarrow$ $i_L = I_{L3} + (V_s/L)t$

6.2 ZVS Resonant Converter IX

- Mode 4 ends at time $t = t_4$ when $i_L(t = t_4) = 0 \rightarrow t_4 = (I_o - I_{L3})(L/V_s)$
- I_{L3} is a negative value

Mode 5



Mode 5

- Mode 5: $t_4 < t < t_5$
- Switch S_1 is ON
- Diode D_m is OFF
- Load current I_o flows through the switch

6.2 ZVS Resonant Converter XI

- Mode 5 ends at time $t = t_5$, when switch S_1 is turned OFF again and the cycle is repeated
- $t_5 = T - (t_1 + t_2 + t_3 + t_4)$
- Peak switch voltage $V_{T(pk)}$ is dependent on the load current I_o $\rightarrow$ Wide variation in the load current results in a wide variation of the switch voltage $\rightarrow$ ZVS converters are used only for constant-load applications

6.3 Comparison of ZCS & ZVS Resonant Converters I

- Both ZCS and ZVS techniques require a variable-frequency control to regulate the output voltage
- In ZCS, the switch is required to conduct a peak current which is higher than the load current I_o, by an amount V_d/Z_o
- In the ZVS topology, switch is required to withstand a forward voltage which is higher than V_d, by an amount $Z_o I_o$
- ZCS converters can eliminate the switching losses at turn-OFF and reduce the switching losses at turn-ON
    - Relatively large capacitor is connected across the diode D_m
    - Inverter operation becomes insensitive to the diodes junction capacitance
- Peak switch current in ZCS is much higher than that in a square wave
- ZVS eliminates the capacitive turn-on loss
    - Suitable for high-frequency operation

6.3 Comparison of ZCS & ZVS Resonant Converters II

- For both ZCS and ZVS, the output voltage control can be achieved by varying the frequency
  - ZCS operates with a constant on-time control
  - ZVS operates with a constant off-time control
- ZVS is preferable over ZCS at high switching frequencies
  - Reason is related to the internal capacitances of the switch
  - When the switch turns ON at zero current but at a finite voltage, the charge on the internal capacitance is dissipated in the switch $\rightarrow$ loss becomes significant at very high switching frequencies. However, no such loss occurs if the switch turns on at a zero voltage

References

1. Mohan, Undeland, Robbins, *"Power Electronics Converters Application and Design"*, Wiley-India
2. Muhammad H. Rashid, *"Power Electronics - Circuits, Devices and Applications"*, Pearson Education
3. Abraham Pressman, *"Switching Power supply Design"*, McGraw Hill

Thank You

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