MAR ATHANASIUS COLLEGE OF ENGINEERING (Autonomous)

Kothamangalam 686 666

Affiliated to APJ Abdul Kalam Technological University

Thiruvananthapuram

Master of Technology (M. Tech.) Curriculum - 2026

VLSI and Embedded Systems

COLLEGE VISION AND MISSION

VISION

Excellence in education through resource integration.

MISSION

The institution is committed to transform itself into a centre of excellence in Technical Education upholding the motto "Knowledge is Power."
This is to be achieved by imparting quality education to mould technically competent professionals with moral integrity, ethical values and social commitment, and by promoting innovative activities in the thrust areas emerging from time to time.

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS)
M.TECH CURRICULUM 2026
Electronics and Communication Engineering
VLSI and Embedded Systems

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PROGRAM OUTCOMES – PO

Outcomes are the attributes that are to be demonstrated by a graduate after completing the program

PO1: An ability to independently carry out research/investigation and development work in engineering and allied streams

PO2: An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.

PO3: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PO4: An ability to apply stream knowledge to design or develop solutions for real world problems by following the standards

PO5: An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tool to model, analyse and solve practical engineering problems.

PO6: An ability to engage in life-long learning for the design and development of the stream related problems taking into consideration sustainability, societal, ethical and environmental aspects. Also to develop cognitive skills for project management and finance which focus on Industry and Entrepreneurship.

The departments conducting the M.Tech program shall define their own PSOs, if required, and evaluation shall also be done for the same.

SEMESTER I

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M26EC1D101	**Discipline Core** CMOS Digital VLSI Design	60	40	3-0-3-6	6	5
B	M26EC1D102	**Programme Core** FPGA-Based System Design	60	40	3-0-3-6	6	5
C	M26EC1T103	**Programme Core** Analog VLSI Design	60	40	4-0-0-5	4	4
D	M26EC1E104A	**Programme Elective 1**	60	40	4-0-0-5	4	4
J	M26GE1R105	**Research Methodology & IPR**	60	40	2-0-0-4	2	2
Total			300	200		22	20

Programme Elective 1

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
D	M26EC1E104A	Embedded Networks	60	40	4-0-0-5	4	4
	M26EC1E104B	Embedded Operating System	60	40	4-0-0-5	4	4
	M26EC1E104C	Semiconductor Memories	60	40	4-0-0-5	4	4
	M26EC1E104D	Machine Learning on Embedded Systems	60	40	4-0-0-5	4	4

Teaching Assistance: 8 hours/week

Self-study- 26 Hrs.

SEMESTER II

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M26EC1D201	**Discipline Core** Design with Advanced Microcontroller	60	40	3-0-3-6	6	5
B	M26EC1D202	**Programme Core**	60	40	3-0-3-6	6	5

		Design of Power supplies and power conversion systems					
C	M26EC1E203A	**Programme Elective 2**	60	40	4-0-0-5	4	4
E	M26EC1S204	**Industry Integrated Course** Embedded Hardware and Interfacing	60	40	4-0-0-5	4	4
G	M26EC1P205	**Mini project**	100		0-0-4-6	4	2
TOTAL			340	160		24	20

Programme Elective 2

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
C	M26EC1E203A	Advanced Digital System Design	60	40	4-0-0-5	4	4
	M26EC1E203B	Sensor Technologies and MEMS	60	40	4-0-0-5	4	4
	M26EC1E203C	Low Power VLSI	60	40	4-0-0-5	4	4
	M26EC1E203D	Embedded systems for IoT applications	60	40	4-0-0-5	4	4

Teaching Assistance: 8 hours/week

Self-study- 28 Hrs.

SEMESTER III

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
A	M26EC1M301	*MOOC	To be completed successfully		--	--	2
K	M26EC1I302	Internship	50	50	--	--	10
P	M26EC1P303	Dissertation Phase 1	100	--	0-0-12-18	12	8
TOTAL			150	50		12	20

Teaching Assistance: 8 hours/week

*MOOC Course of minimum 8 weeks duration to be successfully completed before the end of fourth semester (starting from semester 1).

Internship - mandatory internship of minimum 16 weeks duration.

Dissertation Phase 1 may be undertaken either in the college or in the industry. Dissertation Phase 1 can be linked with internship. Students are expected to have the following skills: Technical Skills, Research Skills, Communication Skills, Critical Thinking Skills, and Problem-Solving Skills.

SEMESTER IV

Slot	Course Code	Courses	Marks		L-T-P-S	Hours	Credit
			CIE	ESE			
P	M26EC1P401	Dissertation Phase II	100	100	0-0-24-26	24	20
TOTAL			100	100		24	20
Total credits in all four semesters							**80**

COURSE NUMBERING SCHEME

The course number consists of digits/alphabets. The pattern to be followed is

For General Courses - MYYBBXCSNN
For Elective Courses - MYYBBXCSNNA

- M: MASTERS
- YY: Last two digits of year of regulation
- BB: DEPARTMENT

Sl.No	Department	Course Prefix
01	Civil Engg	CE
02	Computer Science	CS
03	Electrical & Electronics	EE
04	Electronics & Communication	EC
05	Mechanical Engg	ME
06	Any	GE

07	External (Industry/NPTEL etc)	EX

- X : Specialization number
- C : Course Type

  T- Core Course

  E- Elective Course

  R- Research Methodology & IPR

  D- Lab integrated Course

  S- Industry Integrated Course

  I- Internship

  M- MOOC

  P- Project/Dissertation
- S : Semester of Study

  1. Semester 1
  2. Semester 2
  3. Semester 3
  4. Semester 4
- NN: Course sequence number
- A : Elective sequence number - A/B/C/D/E

It is illustrated below: Examples:

M26CE1T103 is a core course of first specialization offered by the Civil Department in semester 1

M26CE1D201 is a lab integrated core course of first specialization offered by the Civil Department in semester 2

M26GE1R106 is Research Methodology & IPR offered in semester 1offered by all Departments

M26EC1E104A is the first subject of Elective 1 of first specialization offered by the EC Department in semester 1.

EVALUATION PATTERN

(i) LAB INTEGRATED COURSES

Evaluation shall only be based on application, analysis or design based questions (for both internal and

end semester examinations).

Continuous Internal Evaluation (CIE) : 60 marks

Theory Evaluation : 30 marks

Self-study (Course based task/Seminar/ Quiz/ Micro project) :10 marks

Test paper 1 :10 marks

Test paper 2 :10 marks

Lab Evaluation : 30 marks

Lab work : 10 marks

Final evaluation Test : 20 marks

(Note: 50% of Module 1, 2 and 3 may be considered for each test)

End Semester Examination (ESE) : 40marks

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions from first three modules, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

(ii) ELECTIVE COURSES/CORE COURSE

Evaluation shall only be based on application, analysis or design-based questions (for both internal and end semester examinations).

Continuous Internal Evaluation : 60 marks

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/Data collection and interpretation/Case study : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination (ESE) : 40marks

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

(iii) RESEARCH METHODOLOGY & IPR

Continuous Internal Evaluation: 60 marks

Self-study (Preparing a review article based on peer reviewed original publications in the relevant discipline (minimum 10 publications shall be referred))	: 10 marks
Course based task/Seminar/Quiz	: 20 marks
Test paper 1 (Module 1 and Module 2)	: 15 marks
Test paper 2 (Module 3 and Module 4)	: 15 marks
End Semester Examination	**: 40 marks**

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question carries 10 marks.

(iv) INTERNSHIP

Internships are educational and career development opportunities, providing practical experience in a field or discipline. They are structured, short-term, supervised placements often focused around particular tasks or projects with defined time scales. An internship may be compensated or non-compensated by the organization providing the internship. The internship has to be meaningful and mutually beneficial to the intern and the organization. It is important that the objectives and the activities of the internship program are clearly defined and understood. The internship offers the students an opportunity to gain hands-on industrial or organizational exposure; to integrate the knowledge and skills acquired through the coursework; interact with professionals and other interns; and to improve their presentation, writing, and communication skills. Internship often acts as a gateway for final placement for many students.

A student shall opt for carrying out the Internship at an Industry/Research Organization or at another institute of higher learning and repute (Academia). The organization for Internship shall be selected/decided by the students on their own with prior approval from the faculty advisor/respective PG Program Coordinator/Guide/Supervisor. Every student shall be assigned an internship Supervisor/Guide at the beginning of the Internship. The training shall be related to their specialization after the second semester for a minimum duration of sixteen weeks. On completion of the course, the student is expected to be able to develop skills in facing and solving the problems experiencing in the related field.

Objectives

- Exposure to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.

- Exposure to the current technological developments relevant to the subject area of training.
- Create conducive conditions with quest for knowledge and its applicability on the job.
- Understand the social, environmental, economic and administrative considerations that influence the working environment.
- Expose students to the engineer's responsibilities and ethics.

Benefits of Internship Benefits to Students

- An opportunity to get hired by the industry/ organization.
- Practical experience in an organizational setting & Industry environment.
- Excellent opportunity to see how the theoretical aspects learned in classes are integrated into the practical world. On-floor experience provides much more professional experience which is often worth more than classroom teaching.
- Helps them decide if the industry and the profession is the best career option to pursue.
- Opportunity to learn new skills and supplement knowledge.
- Opportunity to practice communication and teamwork skills.
- Opportunity to learn strategies like time management, multi-tasking etc in an industrial setup.
- Makes a valuable addition to their resume.
- Enhances their candidacy for higher education/placement.
- Creating network and social circle and developing relationships with industry people.
- Provides opportunity to evaluate the organization before committing to a full time position.

Benefits to the Institute

- Build industry academia relations.
- Makes the placement process easier.
- Improve institutional credibility & branding.
- Helps in retention of the students.
- Curriculum revision can be made based on feedback from Industry/students.
- Improvement in teaching learning process.

Benefits to the Industry

- Availability of ready to contribute candidates for employment.
- Year-round source of highly motivated pre-professionals.
- Students bring new perspectives to problem solving.
- Visibility of the organization is increased on campus.
- Quality candidate's availability for temporary or seasonal positions and projects.

- Freedom for industrial staff to pursue more creative projects.
- Availability of flexible, cost-effective workforce not requiring a long-termemployer commitment.
- Proven, cost-effective way to recruit and evaluate potential employees.
- Enhancement of employer's image in the community by contributing to theeducational enterprise.

Types of Internships

- Industry Internship with/without Stipend
- Govt / PSU Internship (BARC/Railway/ISRO etc)
- Internship with prominent education/research Institutes
- Internship with Incubation centers /Start-ups

Guidelines

- All the students need to go for internship for minimum duration of 16 weeks.
- Students can take mini projects, assignments, case studies by discussing it with concerned authority from industry and can work on it during internship.
- All students should compulsorily follow the rules and regulations as laid by industry.
- Every student should take prior permissions from concerned industrial authority if they want to use any drawings, photographs or any otherdocument from industry.
- Student should follow all ethical practices and SOP of industry.
- Students have to take necessary health and safety precautions as laid bythe industry.
- Student should contact his /her Guide/Supervisor from college on weeklybasis to communicate the progress.
- Each student has to maintain a diary/log book
- After completion of internship, students are required to submit
    - Report of work done
    - Internship certificate copy
    - Feedback from employer / internship mentor
    - Stipend proof (in case of paid internship).

Total Marks 100: The marks awarded for the Internship will be on the basis of (i)Evaluation done by the industry (ii) Internal evaluation & Student's diary (iii) Internship Report and (iv) Comprehensive Viva Voce.

Continuous Internal Evaluation: 50 marks

Internal evaluation & Student's diary- 25 Marks

Evaluation done by the industry - 25 Marks

Student's Diary/ Daily Log: The main purpose of writing daily diary is to cultivate the habit of documenting and to encourage the students to search for details. It develops the students' thought process and reasoning abilities. The students should record in the daily training diary the day to day account of the observations, impressions, information gathered and suggestions given, if any. It should contain the sketches & drawings related to the observations made by the students. The daily training diary should be signed after every day by the supervisor/ in charge of the section where the student has been working. The diary should also be shown to the Faculty Mentor visiting the industry from time to time and got ratified on the day of his visit. Student's diary will be evaluated on the basis of the following criteria:

- Regularity in maintenance of the diary
- Adequacy & quality of information recorded
- Drawings, design, sketches and data recorded
- Thought process and recording techniques used
- Organization of the information.

The format of student's diary

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From ..... To .....

Brief description about the nature of internship:

Day	Brief write up about the Activities carried out: Such as design, sketches, result observed, issues identified, data recorded, etc.
1	
2	
3	

Signature of Industry Supervisor *Signature of Section Head/HR Manager* *Office Seal*

Attendance Sheet

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From ..... To .....

Signature of Industry Supervisor *Signature of Section Head/HR Manager* *Office Seal*

Note:

- Student's Diary shall be submitted by the students along with attendance record and an evaluation sheet duly signed and stamped by the industry to the Institute immediately after the completion of the training.

Month & Year	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...
Month & Year																					
Month & Year																					

- Attendance Sheet should remain affixed in daily training diary. Do not remove or tear it off.
- Student shall sign in the attendance column. Do not mark 'P'.
- Holidays should be marked in red ink in the attendance column. Absent should be marked as 'A' in red ink.

Evaluation done by the industry (Marks 25)

Format for Supervisor Evaluation of Intern

Student Name:_____ Date:_____ Supervisor Name:_____

_____ Designation:_____ Company/Organization: _____

_____

Internship Address: _____ Dates of Internship: From_____ To _

Please evaluate intern by indicating the frequency with which you observed thefollowing parameters:

Parameters	**Marks** Rating (0-10 mark)
Behavior	
Performs in a dependable Manner	
Cooperates with coworkers and supervisor	
Shows interest in work	
Learns quickly	
Shows initiative	
Produces high quality work	
Accepts responsibility	
Accepts criticism	
Demonstrates organizational skills	
Uses technical knowledge and expertise	
Shows good judgment	
Demonstrates creativity/originality	
Analyzes problems effectively	
Is self-reliant	
Communicates well	
Writes effectively	
Has a professional attitude	
Is punctual	
Uses time effectively	

Evaluation marks: 20 Marks

Overall performance of student: 5 Marks

Intern (Tick one) : Needs improvement (0 - 1 mark) / Satisfactory (1-2 mark) /Good (2-3 mark) / Very Good (3-4 mark) / Excellent (4-5 mark)

Signature of Industry Supervisor *Signature of Section Head/HR ManagerOffice Seal*

End Semester Evaluation (External Evaluation): 50 Marks

Internship Report - 25 Marks

Viva Voce - 25 Marks

Internship Report: After completion of the internship, the student should prepare a comprehensive report to indicate what he has observed and learnt in the training period and should be submitted to the

faculty Supervisor. The student may contact Industrial Supervisor/ Faculty Mentor for assigning special topics and problems and should prepare the final report on the assigned topics. Daily diary will also help to a great extent in writing the industrial report since much of the information has already been incorporated by the student into the daily diary. The training report should be signed by the Internship Supervisor, Program Coordinator and Faculty Mentor.

The Internship report (25 Marks) will be evaluated on the basis of following criteria:

- Originality
- Adequacy and purposeful write-up
- Organization, format, drawings, sketches, style, language etc.
- Variety and relevance of learning experience
- Practical applications, relationships with basic theory and concepts taughtin the course

Viva Voce (25 Marks) will be done by a committee comprising Faculty Supervisor, PG Program Coordinator and an external expert (from Industry or research/academic Institute). This committee will be evaluating the internship report also.

(v) INDUSTRY INTEGRATED COURSE

Engineering students frequently aspire to work in areas and domains that are keytopics in the industry. There are concerns by recruiters that skill sets of engineering students did not match with the Industry requirements, especially in the field of latesttopics. In response to their desires, the College has incorporated Industry integrated course in the curriculum.

The evaluation pattern for Industry based electives is as follows:

Continuous Internal Evaluation: 60 marks

Self-study (*Seminar)	:	10 marks
Course based task/Seminar/Data collection and interpretation/Case study	:	20marks
Test paper 1 (Module 1 and Module 2)	:	15 marks
Test paper 2 (Module 3 and Module 4)	:	15 marks

End Semester Examination: 40 marks

The examination will be conducted by the College with the question paper provided by the Industry. The examination will be for 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks. The valuation of the answer scripts shall be done by the expert in the industry handling the course.

(vi) MOOC COURSES

The MOOC course shall be considered only if it is conducted by the agencies namely AICTE/NPTEL/SWAYAM or NITTTR. The MOOC course should have a minimum duration of 8 weeks and the content of the syllabus shall be enough for at least 40 hours of teaching. The course should have a proctored/offline end semester examination. The students can do the MOOC according to their convenience, but shall complete it before the end of fourth semester. The list of MOOC courses will be provided by the concerned BoS if at least 70% of the course content match with the area/stream of study. The course shall not be considered if its content has more than 50% of overlap with a core/elective course in the concerned discipline or with an open elective.

MOOC Course to be successfully completed before the end of fourth semester (starting from semester 1). A credit of 2 will be awarded to all students whoever successfully completes the MOOC course as per the evaluation pattern of the respective agency conducting the MOOC.

(vii) MINIPROJECT

Total marks: 100

Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The ultimate aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem-solving skills. The introduction of mini projects ensures preparedness of students to undertake dissertation. Students should identify a topic of interest in consultation with PG Program Coordinator. Demonstrate the novelty of the project through the results and outputs. The progressof the mini project is evaluated based on three reviews, two interim reviews and a final review. A report is required at the end of the semester.

Interim evaluation: 60 (30 marks for each review), final evaluation by a Committee(will be evaluating the level of completion and demonstration of functionality/specifications, clarity of presentation, oral examination, work knowledge and involvement): 25, Report (the committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level is not more than 25%): 10, Supervisor/Guide: 5

(viii) DISSERTATION

Dissertation: All Students should carry out the dissertation in the college or can work either in any CSIR/Industrial R&D organization/any other reputed Institute which have facilities for dissertation work in the area proposed.

Dissertation outside the Institute: For doing dissertation outside the Institution, the following conditions are to be met:

- They have completed successfully the course work prescribed in the approved curriculum up to the second semester.
- The student has to get prior approval from the DLAC and CLAC.
- Facilities required for doing the dissertation shall be available in the Organization/Industry (A certificate stating the facilities available in the proposed organization and the time period for which the facilities shall be made available to the student, issued by a competent authority from the Organization/Industry shall be submitted by the student along with the application).
- They should have an external as well as an internal supervisor. The internal supervisor should belong to the parent institution and the external supervisor should be Scientists or Engineers from the Institution/Industry/ R&D organization with which the student is associated for doing the dissertation work. The external supervisor shall be with a minimum post graduate degree in the related area.
- The student has to furnish his /her monthly progress as well as attendance report signed by the external guide and submit the same to the concerned Internal guide.
- The external guide is to be preferably present during all the stages of evaluation of the dissertation.

Note1- Students availing this facility should continue as regular students of the College itself.

Internship leading to Dissertation: The M. Tech students who after completion of 16 weeks internship at some reputed organizations are allowed to continue their work as dissertation for the third and fourth semester after getting approval from the DLAC. Such students shall make a brief presentation regarding the work they propose to carry out before the DLAC for a detailed scrutiny and to resolve its suitability for accepting it as an M.Tech dissertation. These students will be continuing as regular students of the Institute in third semester for carrying out all academic requirements as per the curriculum/regulation. However, they will be permitted to complete their dissertation in the Industry/Organization (where they have successfully completed their internship) during fourth semester.

Dissertation as part of Employment: Students may be permitted to discontinue the program and take up a job provided they have completed all the courses till second semester (FE status students are not permitted) prescribed in the approved curriculum. The dissertation work can be done during a later period either in the organization where they work if it has R & D facility, or in the Institute. Such students should submit application with details (copy of employment offer, plan of completion of their project etc.) to the Dean (PG) through HoD. When the students are planning to do the dissertation work in the organization with R & D facility where they are employed, they shall submit a separate application having following details:

- Name of R&D Organization/Industry
- Name and designation of an external supervisor from the proposed Organization/Industry (Scientists or Engineers with a minimum post graduate degree in the related area) and his/her profile with consent
- Name and designation of a faculty member of the Institute as internal supervisor with his/her consent

- Letter from the competent authority from the Organization/Industry granting permission to do the dissertation
- Details of the proposed work
- Work plan of completion of project

DLAC will scrutinize the proposal and forward to the Dean (PG) through HoD for approval.

When students are doing dissertation work along with the job in the organization (with R & D facility) where they are employed, the dissertation work shall be completed in four semesters normally (two semesters of dissertation work along with the job may be considered as equivalent to one semester of dissertation work at the Institute). Extensions may be granted based on requests from the student and recommendation of the supervisors such that he/she will complete the M. Tech program within four years from the date of admission as per the regulation. Method of evaluation and grading of the dissertation will be the same as in the case of regular students. MOOC can be completed as per the norms mentioned earlier.

Extended Submission for PG Thesis/Project: An extended submission may be permitted for students who have registered for the dissertation/thesis but require additional time for completion. The extended submission period shall be limited to a maximum of three months from the scheduled date of normal submission. Evaluation of theses submitted during the extended period shall be treated as part of the regular examination, and not as a supplementary examination. An extended submission shall be permitted only on the recommendation of the Project Supervisor. If the attendance requirements are not met, an 'FE' grade shall be awarded.

Mark Distribution:

Phase 1: Total marks: 100, only CIE
Phase 2: Total marks: 200, CIE = 100 and ESE = 100 marks

- If the student publishes the dissertation work in a recognized national/international conference or an indexed journal, 10 marks should be awarded.
- Maximum grade (S grade) for the dissertation phase II will be awarded, preferably if the student publishes the dissertation work in an indexed journal
- Final Evaluation (ESE) should be done by a three-member committee comprising the Department Project coordinator, the Guide and an External expert. The external expert shall be an academician or from industry
- If the quantum of work done by the candidate is found to be unsatisfactory, the evaluation committee may extend the duration of the project up to a maximum of three months, giving reasons for this in writing to the student. Normally, further extension will not be granted, and there shall be no provision to register again for the project. A separate evaluation may be conducted for such candidates

(ix) TEACHING ASSISTANTSHIP (TA)

All M.Tech students, irrespective of their category of admission, shall undertake TA duties for a minimum duration as per the curriculum. Being a TA, the student will get an excellent opportunity to improve their expertise in the technical content of the course, enhance communication skills, obtain a hands-on experience in handling the experiments in the laboratory and improve peer interactions.

The possible TA responsibilities include the following: facilitate a discussion section or tutorial for a theory/ course, facilitate to assist the students for a laboratory course, serve as a mentor for students, and act as the course web-master. TAs may be required to attend the instructor's lecture regularly. A TA shall not be employed as a substitute instructor, where the effect is to relieve the instructor of his or her teaching responsibilities.

For the tutorial session:

(i) Meet the teacher and understand your responsibilities well in advance, attend the lectures of the course for which you are a tutor, work out the solutions for all the tutorial problems yourself, approach the teacher if you find any discrepancy or if you need help in solving the tutorial problems, use reference text books, be innovative and express everything in English only.

(ii) Try to lead the students to the correct solutions by providing appropriate hints rather than solving the entire problem yourself, encourage questions from the students, lead the group to a discussion based on their questions, plan to ask them some questions be friendly and open with the students, simultaneously being firm with them.

(iii) Keep track of the progress of each student in your group, give periodic feedback to the student about his/her progress, issue warnings if the student is consistently under-performing, report to the faculty if you find that a particular student is consistently underperforming, pay special attention to slow-learners and be open to the feedback and comments from the students and faculty.

(iv) After the tutorial session you may be required to grade the tutorials/assignments/tests. Make sure that you work out the solutions to the questions yourself, and compare it with the answer key, think and work out possible alternate solutions to the same question, understand the marking scheme from the teacher. Consult the teacher and make sure that you are not partial to some student/students while grading. Follow basic ethics.

Handling a laboratory Session:

(i) Meet the faculty – in- charge a few days in advance of the actual lab class and get the details of the experiment, get clarifications from him/her regarding all aspects of the experiment and the expectations, prepare by reading about the theoretical background of the experiment, know the physical concepts involved in the experiment, go to the laboratory and check out the condition of the equipment/instrumentation, perform the laboratory experiment at least once one or two days before the actual laboratory class, familiarize with safety/ security aspects of the experiment / equipment/laboratory, prepare an instruction sheet for the experiment in consultation with the faculty, and keep sufficient copies ready for distribution to students for their reference.

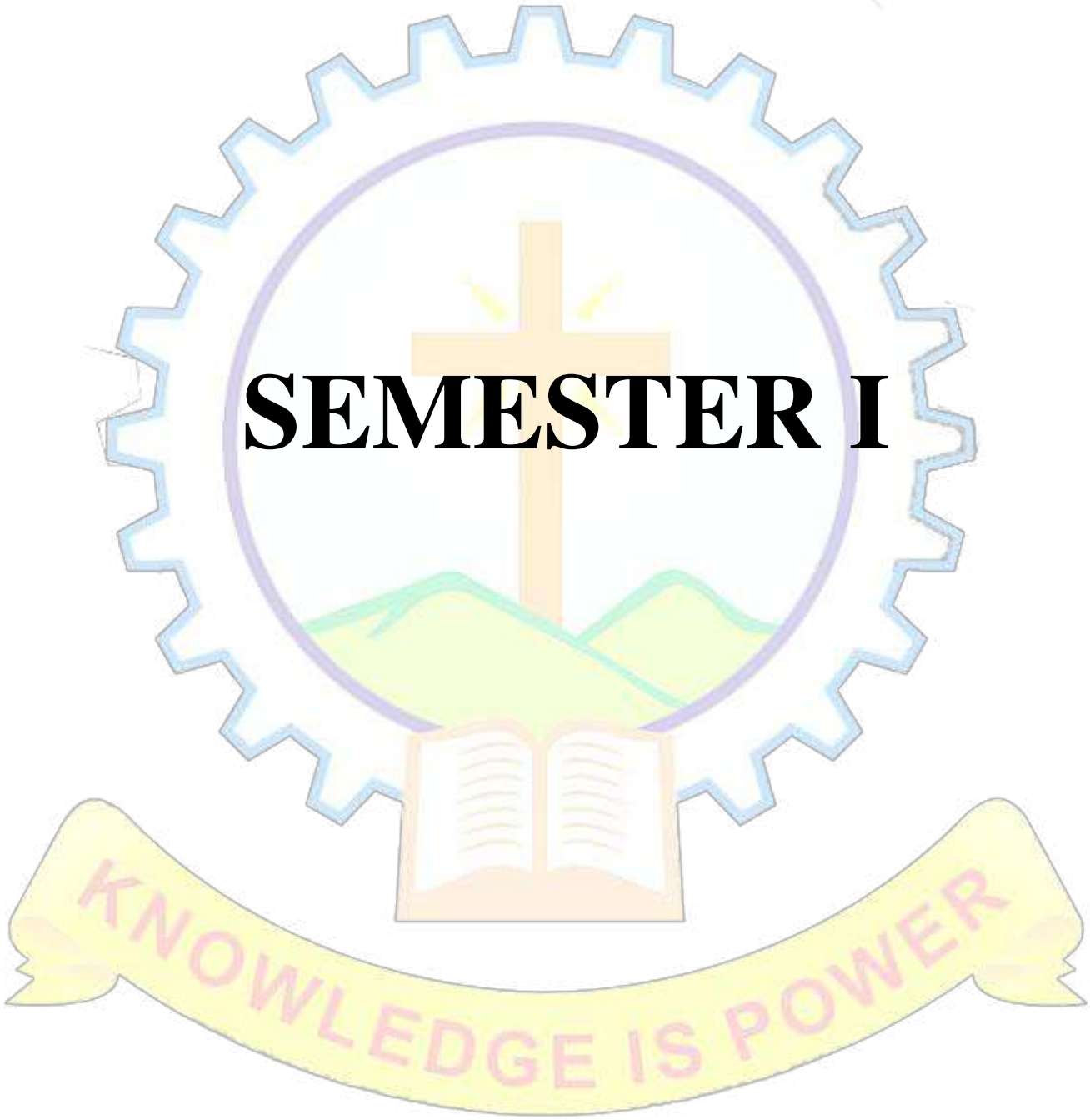
(ii) Verify condition of the equipment/set up about 30 minutes before the students arrive in the class and be ready with the hand outs, make brief introductory remarks about the experiment, its importance, its relevance to the theory they have studied in the class, ask the students suitable questions to know there level of preparation for the experiment, discuss how to interpret results, ask them comment on the results.

(iii) Correct/evaluate/grade the submitted reports after receiving suitable instructions from the faculty in charge, continue to interact with students if they have any clarifications regarding any aspect of the laboratory session, including of course grading, Carefully observe instrument and human safety in

laboratory class, Preparing simple questions for short oral quizzing during explanation of experiments enables active participation of students, facilitate attention, provides feedback and formative evaluation.

POINTS TO REMEMBER

1. Arrange an awareness program to all M.Tech students on day 1 regarding the curriculum and the regulation.
2. The departments should prepare the list of MOOC courses suitable to their program and encourage the students to complete at the earliest.
3. Make a tie up with industries by the middle of semester for Industry Integrated Course. While choosing the course, it should be ensured that the program is relevant and updated in that discipline. The industry expert handling the course shall be a postgraduate degree holder. The evaluation procedure shall also be clearly explained to them.
4. Each department offering M.Tech program should be careful in selecting t mini project in semester 2.
5. The departments should invite the industries/research organizations during first semester and inform them about the mandatory 16 weeks internship that the students should undergo after their second semester. The possibility of doing their dissertation at the industry shall also be explored. They should also be made aware about the evaluation procedure of the Internships. They may also be informed that it is possible to continue internship provided if it leads to their dissertation. Proposals may be collected from them for allotting to students according to their fields of interest.
6. Make sure that all internal evaluations and the end semester examinations to be conducted by the college are carried out as per the evaluation procedure listed in the curriculum. Any dilution from the prescribed procedure shall be viewed seriously.
7. Teaching assistance shall be assigned to all students as per the curriculum. However, a TA shall not be employed as a substitute instructor, where the effect is to relieve the instructor of his or her teaching responsibilities.
8. The possible TA responsibilities include the following: facilitate a discussion section or tutorial for a theory/ course, facilitate to assist the students for a laboratory course, serve as a mentor for students, and act as the course web-master.



SEMESTER I

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1D101	CMOS Digital VLSI Design	Discipline Core	3	0	3	6	5

Preamble: This lab-integrated course provides advanced transistor-level understanding of CMOS digital circuits, from device physics to full-custom physical design. Students will master schematic design, simulation, layout, parasitic extraction, and verification using open-source tools (LTSpice + Magic VLSI). Emphasis is on performance optimization (delay, power, noise margins, area) and real-world sign-off practices.

Prerequisite: Digital Electronics, Semiconductor Devices, Analog Circuits

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyze MOS device characteristics, CMOS inverter, and static/dynamic logic families with performance metrics (delay, power, noise margins) (Analyse)
CO 2	Optimize combinational and sequential circuits using logical effort, timing analysis, and power reduction techniques (Apply, Evaluate)
CO 3	Implement full-custom layout, perform DRC/LVS/RCX, and characterize VLSI subsystems (memory, arithmetic blocks) (Create)
CO 4	Use EDA tools (LTSpice + Magic VLSI) for complete design flow, including post-layout simulation, STA, and mini-project sign-off (Apply, Create)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	2	3	3	3	2
CO 2	3	2	3	3	3	2
CO 3	3	3	3	3	3	3
CO 4	3	3	3	3	3	3

(3 – Strong, 2 – Moderate, 1 – Weak)

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember	10	10	10
Understand	20	20	20
Apply	30	30	30
Analyse	30	30	30

Bloom's Category	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
Evaluate	10	10	10
Create	-	-	-

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Theory Evaluation : 30 marks

Self-study (Course based task/Seminar/Quiz/Micro project) : 10 marks

Test paper 1 : 10 marks

Test paper 2 : 10 marks

Lab Evaluation : 30 marks

Lab work : 10 marks

Final evaluation Test : 20 marks

(Note: 50% of Module 1, 2 and 3 may be considered for each test)

End Semester Examination Pattern:

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions from first three modules, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (12 hours)

MOS transistor review: Structure, long/short-channel I-V characteristics, capacitances, SPICE models, short-channel effects (velocity saturation, DIBL, hot-carrier), scaling trends. CMOS fabrication: n-well process flow, masking, latch-up prevention, well/substrate biasing. CMOS inverter: DC transfer characteristics (VTC), switching threshold, noise margins, sizing for symmetric operation, static/dynamic power, propagation delay. Static CMOS combinational logic: NAND/NOR/AOI/complex gates, complementary CMOS, pass-transistor & transmission-gate logic, full-adder examples. Stick diagrams, lambda/micron-based layout design rules, Euler path for optimal layout, area estimation.

MODULE 2 (12 hours)

Dynamic CMOS logic: Pre-charge/evaluation, domino logic, charge-sharing, clock feed through, keeper transistors, cascading issues. Sequential elements: TG latch, master-slave edge-triggered flip-flops, bi-stability, setup/hold times, clock skew. Timing analysis: RC models, Elmore delay, logical effort, electrical/parasitic delay, multi-stage buffer sizing for minimum delay. Power dissipation: Dynamic (switching + short-circuit) and static (sub threshold, gate leakage) components, power-delay product. Interconnects: Resistance/capacitance models, distributed RC, crosstalk, repeaters/buffers.

MODULE 3 (12 hours)

Arithmetic building blocks: Adders (ripple-carry, CLA), multipliers (array, Booth). Semiconductor memories: SRAM (6T cell, sense amplifiers, pre-charge), DRAM basics. Physical design flow: Floor-planning, placement, global/detailed routing, DRC/LVS/ERC, RC extraction, sign-off (STA, power analysis). Advanced topics: Low-power techniques (voltage scaling, multi-Vt, clock gating, power gating), variability, FinFET impact on digital design, full-custom vs semi-custom flow.

MODULE 4 (36 lab hours) List of Experiments

(All experiments to be performed using LTSpice for schematic & simulation + Magic VLSI for layout, DRC, LVS, RCX and post-layout verification)

1. **MOS Transistor Characterization** Study I-V and C-V characteristics of NMOS and PMOS transistors. Extract SPICE model parameters and observe short-channel effects.
2. **CMOS Inverter Design & Characterization** Design, simulate (pre-layout and post-layout), and characterize CMOS inverter for VTC, noise margins, propagation delay, and power dissipation. Perform sizing for symmetric operation.
3. **Static CMOS Logic Gates** Design and implement layout of 2-input NAND and NOR gates. Perform DRC, LVS, RC extraction, and post-layout simulation. Compare delay and power with inverter.

4. **Complex Static CMOS Gate** Design a complex gate (AOI or full adder) using static CMOS logic. Draw stick diagram, perform optimal layout using Euler's path, and characterize for delay, power, and area.
5. **Dynamic Logic Circuits** Design and simulate domino logic gate (AND/OR). Study charge-sharing, clock feed-through, and the effect of keeper transistor. Perform post-layout simulation.
6. **Sequential Circuits** Design Transmission Gate (TG) latch and master-slave edge-triggered D flip-flop. Verify setup time, hold time, and clock skew through simulation.
7. **Timing Optimization using Logical Effort** Design a multi-stage buffer chain and optimize it for minimum delay using logical effort method. Compare pre-layout and post-layout results.
8. **SRAM Cell Design** Design and characterize 6T SRAM cell for read/write stability (Static Noise Margin – SNM using butterfly curve). Simulate sense amplifier and measure access time (post-layout).
9. **Mini-Project (Full-Custom Design Flow)** Complete full-custom design of any one of the following:
    - 4-bit ALU
    - 8-bit Ripple Carry Adder / Counter
    - Simple Finite State Machine (FSM)

    Perform schematic design, layout, DRC/LVS/RCX, post-layout simulation, timing analysis, power estimation, and generate final GDSII. Submit a mini-project report with sign-off results.

References

1. Jan M. Rabaey et al., Digital Integrated Circuits: A Design Perspective, 2nd Ed., Pearson, 2003.
2. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits, 4th Ed., McGraw-Hill, 2015.
3. Neil H.E. Weste & David Money Harris, CMOS VLSI Design, 4th Ed., Pearson, 2011.
4. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 3rd Ed., Wiley-IEEE, 2010

COURSE CONTENTS AND LECTURE SCHEDULE (36 theory hours + 30–45 lab hours)

No	Topic	No. of Lecture/Tutorial hours
	Module 1	**12**
1.1	MOS device physics, short-channel effects & scaling	3
1.2	CMOS fabrication, latch-up & inverter characteristics	4
1.3	Static logic families, stick diagrams & Euler path layout	5
	Module 2	**12**
2.1	Dynamic logic & sequential circuits	4

No	Topic	No. of Lecture/Tutorial hours
2.2	Timing analysis & logical effort sizing	4
2.3	Power dissipation & interconnect modeling	4
	Module 3	**12**
3.1	Arithmetic building blocks & memories	4
3.2	Physical design flow, DRC/LVS/RCX & STA	4
3.3	Low-power techniques, FinFET & advanced topics	4
	Module 4	
4.1	Lab experiments 1–5	10–12
4.2	Lab experiments 6–8	10–12
4.3	Mini-project (full custom flow)	10–12

Model Question Paper

QP CODE:……... Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

***Course Code*: M26EC1D101**

***Course Name*: CMOS DIGITAL VLSI DESIGN**

Max. Marks: 40 **Duration**: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Derive the expression for the switching threshold voltage (V_M) of a CMOS inverter. Explain how transistor sizing is done to achieve symmetric voltage transfer characteristics (VTC). (5 marks)

   b. With the help of a neat diagram, explain the n-well CMOS fabrication process flow and discuss any two latch-up prevention techniques. (5 marks)

2. a. Draw the stick diagram and explain the Euler path method for obtaining an optimal layout of a complex static CMOS gate (e.g., AOI22 or OAI22). (5 marks)

   b. Discuss the short-channel effects in MOS transistors (Velocity saturation, DIBL, and Hot-carrier effect) and their impact on the performance of digital CMOS circuits. (5 marks)

3. a. Explain the working of Domino logic with suitable waveforms. Discuss the problems of charge sharing and clock feed-through in dynamic logic and how a keeper transistor helps to mitigate them. (6 marks)

   b. Calculate the logical effort (g), electrical effort (h), and parasitic delay (p) for a 2-input NAND gate driving an identical gate. (4 marks)

4. a. Derive the expression for propagation delay using the RC model and Elmore delay for a chain of inverters. Explain the concept of logical effort for multi-stage buffer sizing to achieve minimum delay. (6 marks)

   b. Discuss the various components of power dissipation in CMOS circuits (dynamic switching, short-circuit, and static subthreshold leakage). (4 marks)

5. a. Draw the schematic of a 6T SRAM cell. Explain the read and write operations and derive the Static Noise Margin (SNM) using the butterfly curve. (6 marks)

   b. Compare Ripple-Carry Adder and Carry Look-Ahead (CLA) Adder with respect to delay, area, and power consumption. (4 marks)

6. a. Explain the complete physical design flow in full-custom VLSI design from floor-planning to GDSII sign-off. Highlight the importance of DRC, LVS, and RC extraction. (5 marks)

   b. Discuss any three low-power design techniques (voltage scaling, multi-Vt, clock gating, or power gating) and their impact on performance and power. (5 marks)

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1D102	FPGA Based System Design	Programme Core	3	0	3	6	5

Preamble: The purpose of this course is to introduce basic concepts of FPGA based system design and to impart practical skills in developing a synthesizable digital sub system using Verilog HDL.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design RT-level combinational and regular sequential circuits (Cognitive Knowledge Level: Create)
CO 2	Construct FSM and FSMD (Cognitive Knowledge Level: Analyse)
CO 3	Analyze and implement UART subsystems in FPGA (Cognitive Knowledge Level: Evaluate)
CO 4	Design and implement digital hardware modules using HDL, including combinational, sequential, memory, communication, and display subsystems, and verify their functionality through software simulation and hardware implementation.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	0	3	2	2	0
CO 2	1	0	3	2	2	0
CO 3	2	1	3	3	3	1
CO 4	1	0	3	3	3	1

Assessment Pattern

Bloom's Category	FPGA Based System Design		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	60	60	60
Analyse	20	20	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Theory Evaluation : 30 marks

Self-study (Course based task/Seminar/ Quiz/ Micro project) :10 marks

Test paper 1 :10 marks

Test paper 2 :10 marks

Lab Evaluation : 30 marks

Lab work : 10 marks

Final evaluation Test : 20 marks

(Note: 50% of Module 1, 2 and 3 may be considered for each test)

End Semester Examination Pattern:

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions from first three modules, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Verilog HDL – Introduction, General description, Basic lexical elements and data types, Structural description, Gate-level combinational circuit, Testbench, RT-level combinational circuit and Regular sequential circuit: Introduction, Operators, Always block for a combinational circuit, if statement, Case statement, Parameter and constant, Design examples: shift register, Binary counters, Test bench for sequential circuits, Case study.

MODULE 2 (10 hours)

FSM: Introduction, FSM representation and code development, Mealy and Moore outputs, design examples. FSMD-Introduction, ASMD chart, Code development of an FSMD, Design examples.

MODULE 3 (10 hours)

Implementation of UART sub system: Introduction, UART receiving subsystem, UART transmitting subsystem, Overall UART system, Full-featured UART, UART with an automatic baud rate detection circuit, UART with an automatic baud rate and parity detection circuit, UART-controlled stopwatch, UART-controlled rotating LED banner.

MODULE 4 (30 hours)

List of experiments

1. Write HDL codes to realize multiplexers, encoders and decoders using software simulation.
2. Write HDL codes to design different types of shift registers and demonstrate it using software simulation.
3. Write HDL codes to design different types of binary counters and demonstrate it using software simulation.
4. Write HDL codes to design an 8-bit ALU using software simulation.
5. Write HDL codes to design a controller for 4*4 LED matrix and demonstrate it using software simulation and hardware implementation.
6. Write HDL codes to design an 8-bit RAM using software simulation.
7. Write HDL codes to design and implement a Moore based rising edge detector and demonstrate it using software simulation.
8. Write HDL codes to design and implement a UART transmitter and demonstrate it using software simulation and hardware implementation.

9. Write HDL codes to design and implement a PWM module and demonstrate it using software simulation and hardware implementation.
10. Write HDL codes to design and implement a VGA controller and display lines, rectangles and circles and demonstrate it using software simulation and hardware implementation.

Reference Books

1. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008
2. FPGA-Based System Design – Wayne Wolf, Verlag: Prentice Hall
3. Modern VLSI Design: System-on-Chip Design (3rdEdition) Wayne Wolf, Verlag
4. Field Programmable Gate Array Technology- S. Trimberger, Edr, 1994, Kluwer Academic
5. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall
6. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Second Edition, Prentice Hall PTR, 2003
7. B. Bala Tripura Sundari, T. R. Padmanabhan, "Design Through Verilog HDL", Wiley India, 2012

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction to **Verilog HDL**, design flow, HDL vs schematic design, applications in FPGA and ASIC	1
1.2	**General description of Verilog**, modules, ports, hierarchy, simulation vs synthesis concepts	1
1.3	**Basic lexical elements and data types** – identifiers, numbers, operators, wire, reg, parameters, constants	1
1.4	**Structural description** – module instantiation, interconnections, gate primitives	1
1.5	**Gate-level combinational circuit design** – AND, OR, multiplexers, simple design examples	1
1.6	**Testbench fundamentals** – stimulus generation, $monitor, $display, simulation workflow	1
1.7	**RT-level combinational circuit design** – continuous assignments, operators, always block for combinational circuits	1
1.8	**Decision statements** – if statement, case statement, parameterized design	1
1.9	**Regular sequential circuits** – registers, **shift registers**, **binary counters**, clocked always blocks	1

1.10	**Testbench for sequential circuits** and **case study** (complete RTL design example with simulation)	1
	Module 2	
2.1	Introduction to **Finite State Machines (FSM)**, need for FSM in digital systems, applications in controllers and communication systems	1
2.2	**FSM representation methods** – state diagrams, state tables, state transition concepts	1
2.3	**FSM code development in Verilog** – state encoding, state registers, next-state logic	1
2.4	**Mealy and Moore FSM models** – differences, timing behavior, advantages and disadvantages	1
2.5	Design examples of FSM – sequence detector, traffic light controller	1
2.6	Introduction to **FSMD (Finite State Machine with Datapath)** – need and architecture	1
2.7	**ASMD chart** – concept, symbols, relation between FSM and data path operations	1
2.8	**Code development of FSMD in Verilog** – control unit and data path implementation	1
2.9	**FSMD design examples** – arithmetic controller / serial multiplier/data processing controller	1
2.10	**Case study and design discussion** – complete FSM/FSMD-based system design	1
	Module 3	
3.1	Introduction to UART communication, asynchronous serial communication, frame format (start bit, data bits, parity, stop bit), baud rate	1
3.2	**UART receiver subsystem – basic principles**, sampling methods, start bit detection	1
3.3	**UART receiver design and implementation** in FPGA/Verilog	1
3.4	UART transmitter subsystem – architecture and operation	1
3.5	**UART transmitter implementation** in FPGA/Verilog	1
3.6	**Overall UART system integration** – connecting transmitter and receiver, testing and simulation	1
3.7	**Full-featured UART** – buffering, parity generation/checking, status registers	1
3.8	**UART with automatic baud rate detection circuit** – principle and implementation	1
3.9	UART with automatic baud rate and parity detection circuit	1
3.10	Application examples – UART-controlled stopwatch and UART-controlled rotating LED banner	1
	Module 4	
4.1	Write HDL1 codes to realize multiplexers, encoders and decoders using software simulation.	3
4.2	Write HDL codes to design different types of shift registers and demonstrate it using software simulation.	3
4.3	Write HDL codes to design different types of binary counters and demonstrate it using software simulation.	3

4.4	Write HDL codes to design an 8-bit ALU using software simulation.	3
4.5	Write HDL codes to design a controller for 4*4 LED matrix and demonstrate it using software simulation and hardware implementation.	3
4.6	Write HDL codes to design an 8-bit RAM using software simulation.	3
4.7	Write HDL codes to design and implement a Moore based rising edge detector and demonstrate it using software simulation.	3
4.8	Write HDL codes to design and implement a UART transmitter and demonstrate it using software simulation and hardware implementation.	3
4.9	Write HDL codes to design and implement a PWM module and demonstrate it using software simulation and hardware implementation.	3
4.10	Write HDL codes to design and implement a VGA controller and display lines, rectangles and circles and demonstrate it using software simulation and hardware implementation.	3

Model Question Paper

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Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1D102**

Course Name: **FPGA-BASED SYSTEM DESIGN**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Explain the Verilog HDL design flow used for digital system development targeting FPGA or ASIC.

   Discuss the following aspects:

   - Difference between HDL-based design and schematic-based design
   - Role of simulation and synthesis in the design process
   - Importance of modules, ports and hierarchical design in Verilog.

   b. Write a Verilog RTL description for a 4-to-1 multiplexer using an always block and a case statement. Explain how the operators and data types (wire, reg) are used in the design.

2. a. Write a Verilog code for a 4-bit shift register using a clocked always block. Explain how sequential logic is implemented in RTL modeling.

   b. A student wrote the following Verilog code for a combinational circuit:

```
always @ (a or b or sel)
begin
   if(sel)
        y = a;
```

```
    else
        y = b;
end
```

Analyse the code and answer the following:

- Identify the type of circuit implemented.
- Explain the role of the always block and sensitivity list.
- Suggest how the same function can be implemented using continuous assignment.

3. a. Explain the concept of a Finite State Machine (FSM) and its importance in digital system design.

Discuss the following:

- Need for FSM in controllers and communication systems
- FSM representation methods such as state diagrams and state tables
- Basic state transition concepts

b. Design a sequence detector FSM to detect the input sequence 1011 (overlapping allowed).

- Draw the state diagram
- Develop the state table
- Explain whether the design is Mealy or Moore

4. a. Compare Mealy and Moore FSM models with respect to:

- Output generation
- Timing behavior
- Hardware complexity
- Advantages and disadvantages in practical systems

b. Explain the FSMD (Finite State Machine with Datapath) architecture.

- Describe the ASMD chart and its symbols
- Explain how the control unit and datapath interact
- Illustrate with an example such as a serial multiplier or arithmetic controller

5. a. Explain the UART communication protocol used in asynchronous serial communication.

   Discuss the following:

   - Frame format including start bit, data bits, parity bit, and stop bit
   - Concept of baud rate and bit timing
   - Basic operation of UART transmitter and receiver subsystems

   b. Describe the architecture and operation of a UART transmitter.

   Write a Verilog HDL module for a UART transmitter and explain how data bits are serialized and transmitted using start and stop bits.

6. a. Explain the design of a UART receiver subsystem.

   Discuss the following aspects:

   - Start bit detection
   - Sampling methods for data recovery
   - Implementation considerations in FPGA/Verilog

   b. Explain how a full-featured UART system can be implemented in FPGA.

   Discuss the role of:

   - Buffer registers and status registers
   - Parity generation and checking
   - Automatic baud rate detection circuits
   - Illustrate with an application example such as a UART-controlled stopwatch or rotating LED banner.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1T103	Analog VLSI Design	Programme Core	4	0	0	5	4

Preamble: The Analog VLSI Design course focuses on developing the knowledge and analytical skills required for designing and analyzing CMOS analog circuits. The student will gain an in-depth knowledge in the operation of MOS transistors, acquire the knowledge of the analysis and design of CMOS circuit including basic building blocks of CMOS circuits, amplifiers etc. The student will gain a glance in to the operation and design of advanced circuits.

Prerequisite: NIL

Course Outcomes: After the completion of the course the student will be able to

CO 1	To the understand operation of MOSFET, IV Characteristics, small signal and large signal models and perform analysis.
CO 2	Ability to analyze and design basic analog components including single stage amplifiers and current mirrors.
CO 3	Ability to analyze and understand frequency response and noise sources in circuits
CO 4	Ability to design and analyze various single and multi stage operational amplifiers

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	1	2	2	3	1
CO 2	2	2	2	3	3	1
CO 3	2	2	2	3	3	1
CO 4	2	2	2	3	3	1

Assessment Pattern

	Analog VLSI Design		
Bloom's Category	**Continuous Internal Evaluation Tests**		**End Semester Examination (%Marks)**
	Test 1 (%Marks)	**Test 2 (%Marks)**	
Remember			
Understand	40	40	40
Apply	30	30	30
Analyze	30	30	30
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study: 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

MOS I/V Characteristics: Threshold voltage, derivation of I/V characteristics, regions of operation, MOS Transconductance. Second-order effects: Body effect, Channel Length Modulation, Sub-Threshold Conduction. MOS Device Models: MOS device capacitances, MOS large signal model, MOS small signal model-basic, with channel length modulation, with body effect. MOS Scaling Theory MOS Short Channel Effects: Threshold Voltage Variation, Mobility degradation, velocity saturation, Hot carrier effects, Output impedance variation

MODULE 2 (10 hours)

Single Stage Amplifiers: Common Source (CS) amplifier, large signal and small signal behaviour with resistive load, diode connected load and current source load; CS amplifier with source degeneration, Source follower, Common gate stage.

MODULE 3 (10 hours)

Current Mirrors: Analysis and characteristics of Basic Current Mirror and Cascode Current Mirror, Active Current Mirrors: Differential pair (5 transistor OTA) with active load- large and small signal analysis. Differential Amplifiers: Basic Differential Pair-large signal and small signal behavior, Common Mode response Differential Pair with MOS Loads.

MODULE 4 (10 hours)

Opamp Performance parameters
One stage op-amp topologies: characteristics and design of basic one-stage op-amp, telescopic cascode and folded cascode opamp. Two-stage Opamps: analysis and design of basic two stage topology and two stage. Telescopic cascode topology. Common mode feedback (CMFB): basic concept Common mode sensing in single stage opamp: (resistive feedback, source follower) CMFB feedback techniques in single stage opamp.

Reference Books

1. Behzad Razavi: Design of Analog CMOS Integrated Circuits, Tata McGraw Hill, 2nd Edition 2015.
2. Phillip Allen and Douglas Holberg, "CMOS Analog Circuit Design, Oxford University Press, 2002.
3. R. Jacob Baker, CMOS circuit Design Layout and Simulation, 3rd Edition.
4. David. A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
5. Paul B Gray and Robert G Meyer, Analysis and Design of Analog Integrated Circuits 4th Edition.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	MOS I/V Characteristics: Threshold voltage, derivation of I/V characteristics, regions of operation, MOS Transconductance.	2
1.2	Second order effects: Body effect, Channel Length Modulation, Sub Threshold Conduction.	2
1.3	MOS Device Models: MOS device capacitances, MOS large signal model, MOS small signal model-basic, with channel length modulation, with body effect.	3

1.4	MOS Scaling Theory MOS Short Channel Effects: Threshold Voltage Variation, Mobility degradation, velocity saturation, Hot carrier effects, Output impedance variation	3
	Module 2	
2.1	Single Stage Amplifiers: Common Source (CS) amplifier, large signal behavior with resistive load	2
2.2	Single Stage Amplifiers: Common Source (CS) amplifier small signal behavior with resistive load	2
2.3	Common Source (CS) amplifier diode connected load and current source load	3
2.4	CS amplifier with source degeneration Source follower Common gate stage	3
	Module 3	
3.1	Current Mirrors: Analysis and characteristics of Basic Current Mirror and Cascode Current Mirror	2
3.2	Mirror Active Current Mirrors: Differential pair (5 transistor OTA) with active load large and small signal analysis.	2
3.3	Differential Amplifiers: Basic Differential Pair-large signal and small signal behaviour	3
3.4	Common Mode response Differential Pair with MOS Loads	3
	Module 4	
4.1	One stage op-amp topologies: characteristics and design of basic one stage opamp	2
4.2	Telescopic cascode and folded cascode opamp	2
4.3	Two stage Opamps: analysis and design of basic two stage topology and two stage. Telescopic cascode topology.	3
4.4	Common mode feedback (CMFB): basic concept Common mode sensing in single stage opamp: (resistive feedback, source follower) CMFB feedback techniques in single stage opamp	3

Model Question Paper

QP CODE: Pages: 3

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

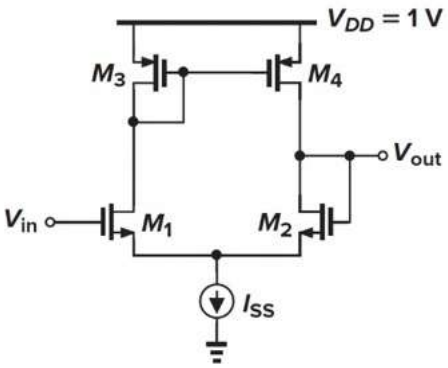
Course Code: M26EC1T103

Course Name: ANALOG VLSI DESIGN

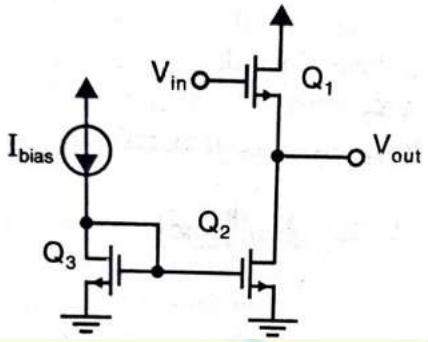
Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Derive the I/V characteristics for a MOSFET in the saturation region.
   b. Explain the channel length modulation and derive the new drain current expressions.
2. a. Compare common source amplifier, common drain amplifier and common gate amplifier with the help of a circuit diagram.
   b. Derive the voltage gain for the common source stage with source degeneration considering body effect and channel length modulation.
3. a. Derive the Common mode gain and common mode rejection ratio of the MOS differential pair.
   b. Derive the voltage gain of the active-loaded MOS differential Pair.
4. a. Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer shown in the circuit below.

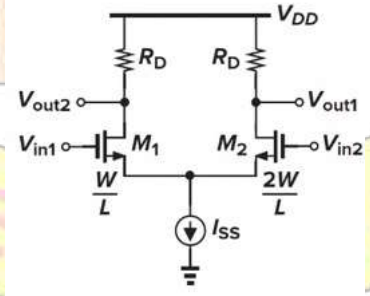


b. Consider the circuit, where all transistors have $\frac{W}{L} = 100\ \mu m/1.6\ \mu m$, $\mu_n C_{ox} = 90\mu A/v^2$, $\mu_p\ C_{ox} = 30\mu A/v^2$, $I_{bias} = 100\mu A$, $\gamma_n = 0.5v^{1/2}$, $r_{ds-n}(\Omega) = \frac{8000L\ \mu m}{I_D\ (mA)}$. What is the gain of the stage.



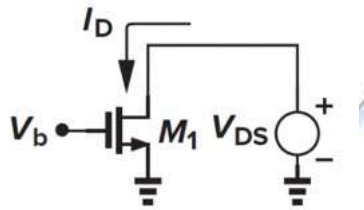
5. a. With the help of a neat diagram derive the voltage gain of a common gate amplifier considering the channel length modulation.

b. Due to a manufacturing error, in the circuit of shown, M_2 is twice as wide as M_1. Calculate the small-signal gain if the dc levels of V_{in1} and V_{in2} are equal.



6. a. With necessary diagram explain the input output characteristics of a differential pair.

b. For the circuit shown, find out the transconductance and plot it as a function of V_{DS}



CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E104A	Embedded Networks	Elective	4	0	0	5	4

Preamble: This course provides a comprehensive transition from simple Chip-to-Chip serial communication to complex Industrial and Wireless Wide Area Networks.

The curriculum is structured to follow the flow of data across different scales: starting with short-range protocols like SPI and I2C, moving into Local Area Networks (Ethernet/TCP-IP), and culminating in high-stakes Industrial Networking (CAN/EtherCAT) and IoT Wireless standards (Wi-Fi/BLE/LoRa).

Prerequisite: Microcontroller and system design, digital communication, C Programming

Course Outcomes: After the completion of the course the student will be able to

CO 1	Analyze and Differentiate between synchronous and asynchronous serial protocols (UART, SPI, I2C) to select the optimal chip-level interface for specific embedded hardware.
CO 2	Implement and Configure LAN parameters including IP addressing, subnetting, and TCP/UDP transport layers based on the OSI and TCP/IP reference models.
CO 3	Evaluate the Determinism and error-management mechanisms of Industrial Networks like CAN and EtherCAT for real-time automation and automotive applications.
CO 4	Compare and Deploy wireless protocol stacks (Wi-Fi, Bluetooth, and LoRaWAN) by assessing trade-offs in range, power consumption, and network topology for IoT solutions.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	1	3	2	3	1
CO 2	2	2	3	3	3	1
CO 3	3	1	3	3	3	1
CO 4	2	2	3	3	3	2

Assessment Pattern

Bloom's Category	Embedded Networks		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember	5	5	5
Understand	20	20	20
Apply	30	30	30
Analyse	30	30	30
Evaluate	10	10	10
Create	5	5	5

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study: 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1: UART, SPI and I2C (10 Hrs)

Embedded Networking basics: Serial/Parallel Communication, Synchronous/Asynchronous Serial Protocols.

Serial communication protocols -UART, RS232, RS485, SPI, I2C

SPI : Introduction, Features, Modes of Operation, External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats)

I2C : I2C-bus features, Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Addressing, Device ID.

MODULE 2 : LAN (10 Hrs)

Introduction to Computer Networks and LAN concepts- LAN Topologies -Ethernet Standards: IEEE 802.3, Fast Ethernet, Gigabit Ethernet -Ethernet Frame Structure and MAC Addressing - Network Devices: Hubs, Switches, Bridges, Repeaters - OSI Reference Model vs TCP/IP Model (layered architecture) - TCP/IP Layers: Application, Transport, Internet, Network Access, TCP and UDP connections - Internet Layer: IP protocol, packet structure, routing basics - IPv4 Addressing: Classes, structure, and notation - Subnetting: Subnet masks, subnet calculation, IPv6 basics and comparison with IPv4 - Network Design: Address planning, subnet allocation

MODULE 3 : Industrial networks (10 Hrs)

Controller Area Network : CAN Overview, Introduction, CAN 2 Standard. Physical Layer, Message Frame Formats, CAN differential signals. CRC mechanism in CAN, Bus Arbitration, Message Reception and Filtering, Error Management, CAN redundancy.

EtherCAT : Introduction to EtherCAT, Determinism, High-speed communication, On-the-fly data processing, Master–Slave concept, EtherCAT frame structure and datagram

Addressing mechanisms: Logical and physical addressing.

MODULE 4 : Wireless Network (10 Hrs)

Wireless networks: Wifi - 802.11 standards, Architecture and protocol stack, Physical layer, MAC sublayer, 802.11 frame structure.

Bluetooth - Architecture, protocol stack - radio layer, link layers, frame structure. Frequency hopping, piconets and scatternets. Bluetooth Low energy (BLE) - Classic Bluetooth vs BLE, BLE Architecture

LoRa Protocol & Communication, LoRaWAN Architecture

References

1. ANDREW S. TANENBAUM, "COMPUTER NETWORKS", FIFTH EDITION, Pearson Education, Inc., publishing as Prentice Hall. 2011
2. Lyla B Das, “Embedded Systems-An Integrated Approach”, Pearson, 2012.
3. Marco Di Natale, Haibo Zeng, Paolo Giusto & Arakadeb Ghosal, “Understanding and Using the Controller Area Network”, Springer, 2012.

4. EtherCAT System Description (Beckhoff), "EtherCAT – The Ethernet Fieldbus" Author: Beckhoff Automation
5. EtherCAT Technology Group (ETG) Compendium, EtherCAT Compendium Publisher: EtherCAT Technology Group
6. LoRa and LoRaWAN for Beginners, Author: M. K.
7. Beginning LoRa Radio Networks with Arduino, Author: Pradeeka Seneviratne

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Embedded Networking basics: Serial/Parallel Communication, Synchronous/Asynchronous Serial Protocols.	1
1.2	Serial communication protocols -UART, RS232, RS485	3
1.3	SPI : Introduction, Features, Modes of Operation, External Signal Description, Functional Description(Covering Master Mode, Slave Mode, Transmission Formats)	3
1.4	I2C : I2C-bus features, Signals and Logic levels, Start/Stop conditions, byte format, Acknowledge and Not-Acknowledge, Clock Synchronization, Arbitration, Addressing, Device ID.	3
	Module 2	
2.1	Introduction to Computer Networks and LAN concepts LAN Topologies	1
2.2	Ethernet Standards: IEEE 802.3, Fast Ethernet, Gigabit Ethernet -Ethernet Frame Structure and MAC Addressing	1
2.3	Network Devices: Hubs, Switches, Bridges, Repeaters	1
2.4	OSI Reference Model vs TCP/IP Model (layered architecture) - TCP/IP Layers: Application, Transport, Internet, Network Access, TCP and UDP connections	1
2.5	Internet Layer: IP protocol, packet structure, routing basics	2
2.6	IPv4 Addressing: Classes, structure, and notation - Subnetting: Subnet masks, subnet calculation, IPv6 basics and comparison with IPv4	2
2.7	Network Design: Address planning, subnet allocation	2
	Module 3	
3.1	Controller Area Network : CAN Overview, Introduction, CAN 2 Standard. Physical Layer, Message Frame Formats, CAN differential signals.	2
3.2	CRC mechanism in CAN, Bus Arbitration, Message Reception and Filtering, Error Management, CAN redundancy.	3
3.3	EtherCAT : Introduction to EtherCAT, Determinism, High-speed communication, On-the-fly data processing, Master–Slave	2

	concept	
3.4	EtherCAT frame structure and datagram	1
3.5	Addressing mechanisms: Logical and physical addressing.	2
	Module 4	
4.1	Wireless networks: Wifi - 802.11 standards, Architecture and protocol stack, Physical layer, MAC sublayer, 802.11 frame structure.	3
4.2	Bluetooth - Architecture, protocol stack - radio layer, link layers, frame structure. Frequency hopping, piconets and scatternets.	3
4.3	Bluetooth Low Energy (BLE) - Classic Bluetooth vs BLE, BLE Architecture	1
4.4	LoRa Protocol & Communication, LoRaWAN Architecture	3

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

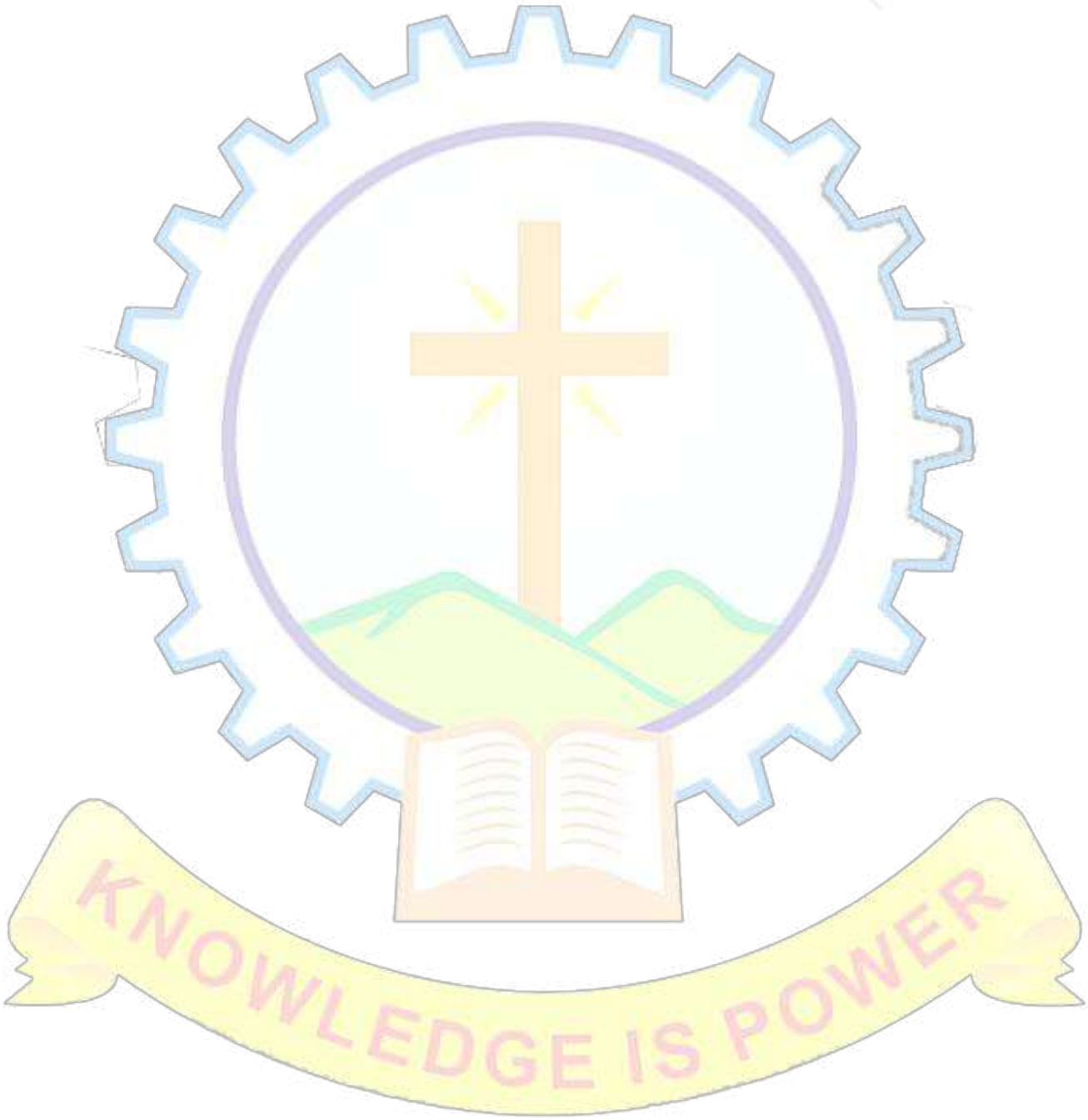
***Course Code*: M26EC1E104A**

***Course Name*: Embedded Networks**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a) Explain synchronous and asynchronous serial communication. Compare UART, SPI, and I2C in terms of architecture, speed, and applications. (5 Marks)
   b) Analyze the SPI protocol in master and slave modes, including signal lines, clock polarity/phase, and data transmission formats. (5 Marks)
2. a) Explain I2C bus features including start/stop conditions, addressing, and acknowledgment mechanism. (5 Marks)
   b) Design an I2C system to interface multiple devices with a microcontroller. Explain how arbitration and clock synchronization ensure reliable communication. (5 Marks)
3. a) Explain LAN topologies and Ethernet standards (IEEE 802.3, Fast Ethernet, Gigabit Ethernet). (5 Marks)
   b) Describe Ethernet frame structure and MAC addressing. Analyze how switches and bridges improve network efficiency. (5 Marks)
4. a) A network with IP 192.168.10.0/24 must be divided into 4 subnets. Determine the subnet mask, subnet addresses, valid host ranges, and broadcast addresses. (5 Marks)
   b) Explain CAN protocol architecture, message frame format, and arbitration mechanism. (5 Marks)
5. a) Analyze error detection and fault confinement techniques in CAN networks. (5 Marks)
   b) Evaluate EtherCAT addressing mechanisms (logical and physical) and frame structure for real-time industrial applications. (5 Marks)
6. a) Analyze MAC layer operation and frame structure in Wi-Fi networks. (5 Marks)
   b) Design a wireless communication system for an IoT application using BLE or LoRaWAN. Justify your choice based on range, power consumption, and network requirements. (5 Marks)


KNOWLEDGE IS POWER

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E104B	Embedded Operating System	Elective	4	0	0	5	4

Preamble: This course introduces operating system fundamentals, real-time system concepts, RTOS task management and scheduling algorithms, and emerging trends in real-time embedded systems including multicore systems, commercial RTOS features, FreeRTOS simulation, and application case studies.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain operating system fundamentals, including kernel architecture, system calls, processes, threads, and CPU scheduling algorithms for understanding task management in computing systems. (Blooms Level: Understand)
CO 2	Analyze real-time system concepts, RTOS architecture, task management, inter-task communication, synchronization, and classical semaphore-based problems to design and manage real-time embedded applications. (Blooms Level: Analyze)
CO 3	Apply real-time scheduling algorithms for periodic and aperiodic tasks, perform schedulability analysis, and resolve priority inversion issues in RTOS-based systems. (Blooms Level: Apply)
CO 4	Examine emerging real-time embedded system technologies, analyze multicore and commercial RTOS features, implement task scheduling and synchronization using FreeRTOS, and understand real-time systems through case studies. (Blooms Level: Analyze)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	1	2	2	1
CO 2	3	2	1	2	2	2
CO 3	3	2	1	2	2	2
CO 4	3	3	3	3	3	3

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	60	60	60
Analyse	20	20	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/Data collection and interpretation/Case study : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Introduction to Operating Systems: Introduction to operating systems, Kernel architecture and functions, Categories of systems, System calls and kernel services, Processes and threads, Process states, state transition and Process Control Block (PCB), Context switching, Process scheduling, Scheduling algorithms - First Come First Serve, Shortest Job First, Smallest Remaining Time First, Priority Based, Round Robin, Multilevel Queue and Multilevel Feedback Queue Scheduling, multiprocessor scheduling. Thread: Structure. User and kernel-level threads, multi-threading models.

MODULE 2 (10 hours)

Introduction to Real Time Systems: Characteristics of real-time systems, Hard, soft and firm real-time systems, RTOS architecture and kernel components, Task management - Task states, Task control block, Task creation and deletion, RTOS scheduling and dispatcher, Inter-task communication mechanisms – Semaphores – Types, Mutex, Message queues, Mailboxes, Pipes, Critical section and resource sharing, Interrupt handling in RTOS, Deadlock management – Detection, Recovery, Avoidance, Prevention, Timer services and clock management, Memory management.
Classical problems in RTOS using semaphores: Producer–Consumer Problem, Readers–Writers Problem, Dining Philosophers Problem.

MODULE 3 (10 hours)

Real Time Scheduling: Real-time scheduling concepts – Task constraints, Aperiodic task scheduling algorithm – Earliest Deadline First algorithm (EDF), Earliest Due Date algorithm, Latest Deadline First algorithm, EDF with precedence constraints, Periodic task scheduling algorithms – Rate Monotonic algorithm, Deadline Monotonic algorithm. Schedulability analysis, Performance metrics, Priority inversion problem - Priority inheritance protocol, Priority ceiling protocol.

MODULE 4 (10 hours)

Emerging Trends in Real Time Embedded Systems: Overview of Embedded Linux and POSIX standards, Real-time communication protocols, Reliability and fault tolerance concepts. Worst-Case Execution Time (WCET) Analysis. Security in real-time embedded systems, Commercial real time operating systems: Features – Free RTOS, MicroC/OS-II, PSOS, VRTX, RT Linux. Multicore real time systems, Load balancing techniques.
Case studies: Real-time systems for automotive, autonomous applications, real-time systems for IoT applications.
Simulation using FREE RTOS: Real time application development using FreeRTOS, Demonstration of - Task creation, Context switching, Priority assignments, Task states, Scheduling of tasks, Semaphore usage.

References

1. Abraham Silberschatz, Operating System Principles, Wiley India
2. William Stallings, Operating systems- Internals and design principles, Prentice Hall
3. Qing Li, Real-Time Concepts for Embedded Systems, CMP Books
4. Andrew S. Tanenbaum, Modern Operating Systems, Pearson
5. Rajib Mall, Real-Time Systems: Theory and Practice, Pearson
6. Raj Kamal, Embedded Systems – Architecture, Programming and Design, Tata McGraw Hill

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction to operating systems, Kernel architecture and functions	1
1.2	Categories of systems, System calls and kernel services	1
1.3	Processes and threads	1
1.4	Process states, state transition and Process Control Block (PCB)	1
1.5	Context switching, Process scheduling	1
1.6	Scheduling algorithms - First Come First Serve, Shortest Job First	1
1.7	Smallest Remaining Time First, Priority Based	1
1.8	Round Robin, Multilevel Queue and Multilevel Feedback Queue Scheduling	1
1.9	Multiprocessor scheduling	1
1.10	Thread: Structure. User and kernel-level threads, multi-threading models	1
	Module 2	
2.1	Characteristics of real-time systems: Hard, soft and firm real-time systems	1
2.2	RTOS architecture and kernel components	1
2.3	Task management - Task states, Task control block, Task creation and deletion	1
2.4	RTOS scheduling and dispatcher, Inter-task communication mechanisms – Semaphores – Types, Mutex	1
2.5	Message queues, Mailboxes	1
2.6	Pipes, Critical section and resource sharing, Interrupt handling in RTOS	1
2.7	Deadlock management – Detection, Recovery, Avoidance, Prevention	1

2.8	Timer services and clock management, Memory management,	1
2.9	Classical problems in RTOS using semaphores: Producer–Consumer Problem	1
2.10	Readers–Writers Problem, Dining Philosophers Problem	1
	Module 3	
3.1	Real-time scheduling concepts – Task constraints	1
3.2	Aperiodic task scheduling algorithm – Earliest Deadline First algorithm (EDF)	1
3.3	Aperiodic task scheduling algorithm – Earliest Deadline First algorithm (EDF)	1
3.4	EDF with precedence constraints	2
3.5	Periodic task scheduling algorithms – Rate Monotonic algorithm	2
3.6	Deadline Monotonic algorithm	1
3.7	Schedulability analysis, Performance metrics	1
3.8	Priority inversion problem - Priority inheritance protocol, Priority ceiling protocol	1
	Module 4	
4.1	Overview of Embedded Linux and POSIX standards	1
4.2	Real-time communication protocols	1
4.3	Reliability and fault tolerance concepts	1
4.4	Worst-Case Execution Time (WCET) Analysis	1
4.5	Security in real-time embedded systems	1
4.6	Commercial real time operating systems: Features – Free RTOS, MicroC/OS-II, PSOS, VRTX, RT Linux	1
4.7	Multicore real time systems, Load balancing techniques	1
4.8	Real-time systems for automotive, autonomous applications, real-time systems for IoT applications	1
4.9	Real time application development using FreeRTOS, Demonstration of - Task creation, Context switching	1
4.10	Priority assignments, Task states, Scheduling of tasks, Semaphore usage	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1E104B**

Course Name: **Embedded Operating System**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Explain process states and transitions between each state. Justify the statement that context switching will significantly improve processor utilization. Explain the significance of the process control block in context switching.

   b. Schedule the tasks according to the Round Robin scheduling algorithm. Assume the time quantum to be 2 ms. Justify the need for an optimal time quantum.

Process	Arrival time (ms)	Burst Time (ms)
P1	0	5
P2	1	3
P3	2	1
P4	3	2
P5	4	3

2. a. Explain the mechanism of achieving synchronization using semaphores. Classify and explain semaphore types and their state transition.

   b. Demonstrate and explain the producer-consumer problem with an example. Justify the use of semaphores in it.

3. a. Illustrate and explain various constraints that need to be taken into account while scheduling real-time tasks. With the help of an example, prove that the EDF algorithm is optimal in minimising the minimum lateness of tasks.

   b. Illustrate and explain the priority inversion problem. Suggest solutions for overcoming this. Differentiate between the rate monotonic and deadline monotonic algorithm with examples.

4. a. With the help of a block diagram, explain real-time requirements and implementation of adaptive cruise control for automotive applications. Explain the functionality of each task and explain the synchronization mechanism between tasks.

   b. Describe WCET analysis and its significance. Describe the features of a free RTOS for handling real-time tasks.

5. a. Demonstrate and explain the dining philosophers' problem. Justify its physical significance in a computing scenario. Illustrate the use of semaphores in solving the problem.

   b. Differentiate between process and thread with examples. What are the different types of threads, and how does it differ in terms of scheduling?

6. a. Given a set of 4 periodic tasks with computation time (Ci) and period (Ti). Schedule the tasks according to Rate Monotonic scheduling. Comment whether all the tasks complete their execution before the deadline.

Task	Ci	Ti
T1	1	4
T2	2	6
T3	1	8

b. Given seven tasks, A, B, C, D, E, F, and G. Construct the precedence graph from the following precedence relations:

A→C; B →C; B→D; C →E; C→F; D→F; D→G

Assuming that all tasks arrive at time t =0, all tasks have a deadline D = 25, and computation times 2, 3, 3, 5, 1, 2, 5, respectively. Modify their arrival times and deadlines to schedule them by EDF with precedence constraints.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E104C	Semiconductor Memories	Elective	4	0	0	5	4

Preamble: This course aims to impart the advance knowledge of memory devices and enable students to Design, test and debug the memory devices.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the architecture, operation, and technological developments of SRAM and DRAM memory systems used in modern semiconductor devices. (Blooms Level: Understand)
CO 2	Analyze the structure, operation, and characteristics of non-volatile memory technologies including ROM, PROM, EPROM, EEPROM, and Flash memories. (Blooms Level: Analyze)
CO 3	Evaluate memory fault models, testing techniques, and design-for-testability approaches used in semiconductor memory systems. (Blooms Level: Evaluate)
CO 4	Assess reliability issues and emerging semiconductor memory technologies, including advanced memory devices and high-density memory packaging techniques. (Blooms Level: Evaluate)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	0	3	1	2	0
CO 2	1	0	3	2	2	0
CO 3	2	0	3	2	3	0
CO 4	2	1	3	2	2	1

Assessment Pattern

Bloom's Category	Semiconductor Memories		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	60	60	60
Analyse	20	20	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

SRAM and DRAM Technologies: Random Access Memory Technologies: Static Random Access Memories (SRAMs): SRAM cell structure, MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, silicon on insulator (SOI) technology, advanced SRAM architectures and technologies, application-specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM technology development, CMOS DRAMs, DRAM cell theory and advanced cell structures, BiCMOS DRAMs, soft error failure in DRAMs, advanced DRAM designs and architectures, application-specific DRAMs.

MODULE 2 (10 hours)

Non-Volatile Memory Technologies: Masked Read Only Memories (ROMs): High density ROMs. Programmable Read Only Memories (PROMs): Bipolar PROMs and CMOS PROMs. Erasable Programmable Read Only Memories (EPROMs): UV-EPROMs, floating gate EPROM cell, one-time programmable (OTP) EPROMs. Electrically Erasable PROMs (EEPROMs): EEPROM technology and architecture, non-volatile SRAM. Flash memories: Flash memory architecture and operation, advanced flash memory architectures.

MODULE 3 (10 hours)

Memory Fault Modelling and Testing: Memory fault modelling and testing. RAM fault modelling and electrical testing techniques. Pseudo-random testing methods. Megabit DRAM testing techniques. Non-volatile memory fault modelling and testing. IDDQ fault modelling and testing. Application-specific memory testing and design for testability (DFT) techniques for memory circuits.

MODULE 4 (10 hours)

Memory Reliability and Advanced Memory Technologies: Semiconductor memory reliability: General reliability issues, RAM failure modes and mechanisms, non-volatile memory reliability, reliability modelling and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification. Advanced memory technologies: Ferroelectric RAM (FRAM), Gallium Arsenide (GaAs) FRAMs, analog memories, magneto-resistive RAM (MRAM), experimental memory devices. High-density memory packaging technologies: Memory hybrids and multi-chip modules (MCMs – 2D), memory stacks and MCMs (3D), memory MCM testing and reliability issues, memory cards and high-density memory packaging, future directions in semiconductor memories.

References

1. Ashok K.Sharma, Semiconductor Memories Technology, testing and reliability, Prentice Hall of India Private Limited, New Delhi, 1997.
2. Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley, 2002.
3. Luecke Mize Care, “Semiconductor Memory design & application”, McGraw-Hill

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction to semiconductor memories and classification of RAM technologies	1
1.2	Static Random-Access Memories (SRAM): basic concepts and SRAM cell structure	1
1.3	MOS SRAM architecture and operation of MOS SRAM cells	1
1.4	Peripheral circuits in SRAM: decoders, sense amplifiers, and write drivers	1
1.5	Bipolar SRAM technologies and Silicon-On-Insulator (SOI) SRAM	1
1.6	Advanced SRAM architectures and application-specific SRAMs	1
1.7	Dynamic Random-Access Memories (DRAM): evolution and technology development	1
1.8	DRAM cell theory and advanced DRAM cell structures	1
1.9	BiCMOS DRAMs and soft error failures in DRAM	1
1.10	Advanced DRAM architectures and application-specific DRAMs	1
	Module 2	
2.1	Introduction to non-volatile memories and ROM technologies	1
2.2	Masked ROM and high-density ROM architectures	1
2.3	Programmable ROM (PROM): bipolar PROM and CMOS PROM	1
2.4	UV-EPROM technology and floating gate EPROM cell	1
2.5	One-Time Programmable (OTP) EPROM and applications	1
2.6	Electrically Erasable PROM (EEPROM): technology and operation	1
2.7	EEPROM architecture and non-volatile SRAM	1
2.8	Flash memory technology and basic flash cell operation	1
2.9	Advanced flash memory architectures	1
2.10	Applications of flash memories and non-volatile memory systems	1
	Module 3	
3.1	Introduction to memory testing and fault modelling	1
3.2	RAM fault modelling techniques	1
3.3	Electrical testing methods for semiconductor memories	1
3.4	Pseudo-random testing techniques	1
3.5	Megabit DRAM testing techniques	1
3.6	Non-volatile memory fault modelling	1

3.7	Non-volatile memory testing techniques	1
3.8	IDDQ fault modelling	1
3.9	IDDQ testing methods for memory circuits	1
3.10	Application-specific memory testing and design-for-testability (DFT)	1
	Module 4	
4.1	Introduction to semiconductor memory reliability	1
4.2	Reliability issues and failure mechanisms in RAM	1
4.3	Reliability challenges in non-volatile memories	1
4.4	Reliability modelling and failure rate prediction	1
4.5	Design for reliability in memory circuits	1
4.6	Reliability test structures	1
4.7	Reliability screening and qualification procedures	1
4.8	Emerging memory technologies: FRAM and GaAs FRAM	1
4.9	Advanced memories: MRAM, analog memories and experimental devices	1
4.10	High-density memory packaging: MCMs, memory stacks and future directions	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1E104C**

Course Name: **Semiconductor Memories**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Explain the structure and operation of an SRAM cell. Discuss the MOS SRAM architecture and the role of peripheral circuits such as decoders and sense amplifiers.

   b. Describe the different SRAM technologies, including bipolar SRAM, SOI technology, and advanced SRAM architectures used in modern semiconductor memories.

2. a. Explain the working of ROM and PROM technologies. Compare bipolar PROM and CMOS PROM implementations.

   b. Describe the floating gate EPROM cell and explain the operation of UV-EPROM and OTP EPROM devices.

3. a. Explain the concept of memory fault modelling. Describe common RAM fault models used in memory testing.

   b. Discuss the electrical testing techniques used for semiconductor memories, including pseudo-random testing methods.

4. a. Explain the testing challenges in megabit DRAM memories and discuss techniques used for DRAM testing.

b. Describe IDDQ fault modelling and testing. Explain how it is used in detecting faults in memory circuits.

5. a. Explain the reliability issues in semiconductor memories. Discuss RAM failure mechanisms and reliability modelling techniques.

   b. Describe the methods used for reliability screening and qualification of memory devices.

6. a. Explain the working principles of emerging memory technologies such as FRAM, MRAM, and analog memories.

   b. Discuss high-density memory packaging techniques, including memory stacks and multi-chip modules (MCMs), and explain their reliability challenges.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1D104D	Machine Learning on Embedded systems	Elective	4	0	0	5	4

Preamble: Machine Learning for Embedded Systems equips students to deploy optimized TinyML models on resource-constrained microcontrollers for real-time edge applications.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to

CO 1	Explain ML fundamentals, pipeline, metrics, and validation techniques across learning paradigms.
CO 2	Implement classical regression/classification algorithms with feature selection and regularisation.
CO 3	Apply clustering, dimensionality reduction, and ensemble methods for data analysis.
CO 4	Design/deploy optimized TinyML models on embedded platforms using Edge Impulse and TFLM

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	2	3	2	2	1
CO 2	2	1	3	3	3	2
CO 3	2	1	3	3	3	2
CO 4	3	2	3	3	3	3

Assessment Pattern

Bloom's Category	Course name		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	10	20
Apply	40	40	40
Analyse	35	40	30
Evaluate	5	10	10

Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study: 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Introduction: Introduction to Machine Learning, Different types of learning- supervised, semi-supervised, unsupervised, reinforcement learning, Hypothesis space and inductive bias, Basic Machine learning pipeline – features, feature vector, training, testing and validation. Evaluation Metrics – accuracy, precision, recall, specificity, FPR, FNR, ROC curve. Cross-validation, Concept of over-fitting, under-fitting, bias-variance trade-off, Regularization, Basics of parameter estimation - maximum likelihood estimation (MLE) and maximum a posteriori estimation (MAP).

MODULE 2 (14 hours)

Regression - Linear regression with one variable, Linear regression with multiple variables, solution using the gradient descent algorithm and matrix method. Linear Methods for Classification- Logistic regression, Probability and Bayes Learning: Bayesian Learning, Decision tree learning: Introduction, Decision tree representation, decision tree algorithm ID3. K nearest neighbour, the Curse of Dimensionality, Feature Selection: forward search, backward search, SVM - Introduction, Maximum Margin Classification, soft margin SVM classifier, non-linear SVM, Kernels for learning non-linear functions, polynomial kernel, Radial Basis Function(RBF).

MODULE 3 (11 hours)

Unsupervised Learning: Clustering – Introduction, Similarity measures, Algorithms: Partitioning methods: K-means, K-medoid, hierarchical methods: agglomerative, BIRCH, Density-based methods: DBSCAN, Expectation maximisation (EM) for soft clustering. Dimensionality reduction – Principal Component Analysis, combining multiple learners: Voting, Ensemble Learning - boosting, bagging, stacking, Random Forest.

MODULE 4 (9 hours)

Introduction to Embedded Machine Learning: End-to-end development of ML applications using Edge Impulse: data collection from sensors, Data pre-processing, feature extraction, feature selection, model training.

Model optimization techniques for embedded ML: quantization, pruning, model size vs performance trade-offs. Hardware constraints and selection criteria for ML deployment. Multi-sensor fusion. Deployment frameworks: TensorFlow Lite, TensorFlow Lite for Microcontrollers (TFLM).

References

1. Ethem Alpaydin, Introduction to Machine Learning, 2nd edition, MIT Press 2010.
2. Kevin P. Murphy, “Machine Learning: A Probabilistic Perspective”, MIT Press, 2012.
3. Pete Warden, Daniel Situnayake, TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers, O’Reilly Media, 2020.
4. Daniel Situnayake, Ian Buckley, Practical TinyML: Deploying Machine Learning on Microcontrollers with TensorFlow Lite, O’Reilly Media, 2022.
5. Christopher Bishop, “Pattern Recognition and Machine Learning” Springer, 2007.
6. Jake VanderPlas, Python Data Science Handbook, O'Reilly Media, 2016
7. Tom Mitchell, Machine Learning, McGraw-Hill, 1997.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction to Machine Learning, Different types of learning- supervised, semi-supervised, unsupervised, reinforcement learning	1
1.2	Hypothesis space and inductive bias	1
1.3	Basic Machine learning pipeline – features, feature vector, training, testing and validation.	1
1.4	Evaluation Metrics – accuracy, precision, recall, specificity, FPR, FNR, ROC curve. Cross-validation,	2
1.5	Concept of over-fitting, under-fitting, Bias-Variance trade off,	2
1.6	Regularization,	1
1.7	Basics of parameter estimation - maximum likelihood estimation (MLE) and maximum a posteriori estimation	2
	Total	10
	Module 2	
2.1	Regression - Linear regression with one variable, Linear regression with multiple variables, solution using the gradient descent algorithm and matrix method.	2
2.2	Linear Methods for Classification- Logistic regression,	2
2.3	Probability and Bayes Learning: Bayesian Learning,	2
2.4	Decision tree learning: Introduction, Decision tree representation, decision tree algorithm ID3.	2
2.5	K nearest neighbour, the Curse of Dimensionality, Feature Selection: forward search, backward search,	2
2.6	SVM - Introduction, Maximum Margin Classification, soft margin SVM classifier,	2
2.7	Non-linear SVM, Kernels for learning non-linear functions, polynomial kernel, Radial Basis Function (RBF).	2
	Total	14

	Module 3	
3.1	Unsupervised Learning: Clustering – Introduction, Similarity measures	1
3.2	Algorithms: Partitioning methods: K-means, K-medoid,	3
3.3	Hierarchical methods: agglomerative, BIRCH,	2
3.4	Density based methods: DBSCAN	1
3.5	Expectation maximization (EM) for soft clustering.	1
3.6	Dimensionality reduction – Principal Component Analysis,	1
3.7	Combining multiple learners: Voting, Ensemble Learning - boosting, bagging, stacking,	1
3.8	Introduction to Random Forest.	1
	Total	11
	Module 4	
4.1	Introduction to Embedded Machine Learning	1
4.2	Development of ML applications using Edge Impulse: data collection from sensors, Data pre-processing, feature extraction, feature selection, model training.	2
4.3	Model optimization techniques for embedded ML: quantization, pruning,	2
4.4	Model size vs performance trade-offs. Hardware constraints and selection criteria for ML deployment.	2
4.5	Multi-sensor fusion.	1
4.6	Deployment frameworks: TensorFlow Lite, TensorFlow Lite for Microcontrollers (TFLM).	1
	Total	9

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1D104D**

Course Name: **Machine Learning on Embedded Systems**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Given the following data, construct the Receiver Operator Characteristic (ROC) curve of the data. Compute the AUC. (6 Mark)

Threshold	TP	TN	FP	FN
1	0	5	0	5
2	1	5	0	4
3	1	4	1	4
4	3	4	1	2
5	3	3	2	2
6	4	3	2	1
7	4	2	3	1
8	4	1	4	1
9	5	0	5	0

b. Distinguish between overfitting and underfitting. How can it affect model generalization? (4 mark)

2. a. State the mathematical formulation of the SVM problem. Give an outline of the method for solving the problem. (5 mark)

   b. Is regression a supervised learning technique? Justify your answer. Compare regression with classification with examples. (5 Mark)

3. a. Identify and explain any three-model combination approach to improve the accuracy of a classifier. (6 mark)

   b. Discuss the importance of the similarity metric in clustering. Why it is difficult to handle categorical data for clustering? (4 mark)

4. a. Explain the complete Edge Impulse end-to-end ML pipeline for sensor-based applications. (5 Mark)

   b. Differentiate post-training quantization from quantization-aware training. Give one advantage each. (5 Mark)

5. a. Explain the general MLE method for estimating the parameters of a probability distribution. (4 Mark)

   b. Using the following dataset given below, Find first Splitting attribute for decision tree by using ID3 algorithm (6 Mark)

Outlook	Temp	Humidity	Windy	Class
Sunny	75	70	True	Play
Sunny	80	90	True	No play
Sunny	85	85	False	No play
Sunny	72	95	False	No play
Sunny	69	70	False	Play
Overcast	72	90	True	Play
Overcast	83	78	False	Play
Overcast	64	65	True	Play
Rainy	81	75	False	Play
Rainy	71	80	True	No Play
Rainy	65	70	True	No Play
Rainy	75	80	False	Play
Rainy	68	80	False	Play

6. a. Given the following distance matrix, construct the dendrogram using single linkage clustering algorithm. (6 Mark)

Item	A	B	C	D	E
A	0	2	3	3	4
B	2	0	3	5	4
C	3	3	0	2	6
D	3	5	2	0	4
E	4	4	6	4	0

b. List 5 model optimization techniques for embedded ML deployment. Briefly explain any two. (4 Marks)

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26GE1R105	Research Methodology & IPR	Theory	2	0	0	4	2

Preamble

Research methodology and intellectual property rights form an essential foundation for postgraduate students and research scholars engaged in advanced engineering studies. This course introduces the principles of scientific research, problem identification, experimental and analytical methods, and effective technical communication. It also emphasizes ethical research practices, scholarly publication processes, and the protection of intellectual property arising from research and innovation. The course aims to equip M Tech students and research scholars with the skills required to conduct systematic research, communicate findings effectively, and understand the legal and ethical frameworks governing intellectual property and technology development.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the principles, processes, and characteristics of scientific research and apply creative and logical thinking approaches for identifying research directions. (Cognitive Knowledge Level: Understand)
CO 2	Apply literature survey techniques and analytical reasoning to identify research gaps and formulate well-defined research problems. (Cognitive Knowledge Level: Apply)
CO 3	Analyze experimental data and develop appropriate experimental or modelling approaches for solving engineering research problems. (Cognitive Knowledge Level: Analyze)
CO 4	Demonstrate effective technical communication while adhering to research ethics and intellectual property regulations. (Cognitive Knowledge Level: Apply)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2		2		1	1
CO 2	3	1	2	1	2	1
CO 3	3		2	2	3	1
CO 4	1	3	2		1	3

Assessment Pattern

Course name	Research Methodology & IPR		
Bloom's Category	**Continuous Assessment Tests**		**End Semester Examination (%Marks)**
	Test 1 (%Marks)	**Test 2 (%Marks)**	
Remember	20		
Understand	40	40	40
Apply	40	40	40

Analyse		20	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Preparing a review article based on peer reviewed original publications in the relevant discipline (minimum 10 publications shall be referred)) : 10 marks

Course based task/Seminar/Quiz : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

End Semester Examination Pattern:

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question carries 10 marks.

MODULE 1: Foundations of Research and Creative Thinking (6 Hours)

Meaning, objectives and significance of research – types of research, basic, applied and interdisciplinary research – characteristics of good research and stages in the research process – skills, habits and attitudes required for researchers – motivation for research with discussion of Richard Hamming's lecture *"You and Your Research"* – thinking skills in research, levels and styles of thinking, common sense versus scientific thinking, logical reasoning and decomposition of complex problems – creativity in research, definitions and characteristics, intelligence versus creativity, creative thinking process and requirements for innovation.

MODULE 2: Literature Survey and Research Problem Formulation (5 Hours)

Importance of literature survey in research – sources of scientific information, journals, conference papers, patents and technical reports – techniques for information search using digital databases – reading, documentation and referencing practices – integration of research literature and identification of research gaps – attributes and sources of research problems – problem formulation and research questions – multiple approaches to solving research problems – techniques for problem representation, graphical methods and reasoning – analytical and analogical reasoning – creative problem solving approaches including TRIZ.

MODULE 3: Experimental Design, Modelling and Data Analysis (8 Hours)

Scientific method and hypothesis formulation – experimental variables, dependent and independent variables, control and reproducibility in experiments – precision, accuracy and measurement errors – random and systematic errors, detection and reduction – statistical treatment and interpretation of experimental data – principles of design of experiments and experimental documentation – modelling in engineering research, types of models and stages in modelling – curve fitting and approximations – mathematical representation and logical reasoning in models – continuum, meso and micro scale modelling approaches – introduction to numerical simulation methods with illustrative case studies.

MODULE 4: Technical Communication, Research Ethics and Intellectual Property Rights (6 Hours)

Importance of effective communication in research – communication process and barriers – oral communication skills for seminars, conferences and project presentations – preparation and delivery of technical presentations – guidelines for effective presentation slides – principles of scientific writing – structure of technical papers, theses and reports – language, layout, typography, tables and figures – referencing and citation styles – tools for document preparation including LaTeX – scholarly publications including journals and conferences – journal selection and peer review process – research metrics – plagiarism, research integrity and ethical publication practices- Introduction to Intellectual Property Rights – types of IPR: patents, copyrights, trademarks and industrial designs – patent concepts, objectives and patentability criteria – patent application procedures and documentation – technology transfer and IPR agreements.

References

1. Panneerselvam, R., *Research Methodology*, PHI Learning, New Delhi.
2. Kothari, C. R. and Garg, G., *Research Methodology: Methods and Techniques*, New Age International.
3. Phillips, E. M. and Pugh, D. S., *How to Get a PhD*, Viva Books.
4. Leedy, P. D. and Ormrod, J. E., *Practical Research: Planning and Design*, Pearson.
5. Day, R. A. and Gastel, B., *How to Write and Publish a Scientific Paper*, Cambridge University Press.
6. Thiel, D. V., *Research Methods for Engineers*, Cambridge University Press.
7. Bouchoux, D. E., *Intellectual Property: The Law of Trademarks, Copyrights, Patents and Trade Secrets*.
8. Resnik, D. B., *The Ethics of Science: An Introduction*, Routledge.
9. Medawar, P., *Advice to a Young Scientist*.
10. Wilson, E. O., *Letters to a Young Scientist*.
11. Hamming, R., *You and Your Research*, Bell Labs Lecture.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
Module 1 (6 Hours)		
1.1	Meaning, objectives and significance of research – types of research: basic, applied and interdisciplinary	1
1.2	Characteristics of good research – stages in the research process	1
1.3	Skills, habits and attitudes required for researchers – motivation for research – discussion of Richard Hamming's lecture "You and Your Research"	1
1.4	Thinking skills in research – levels and styles of thinking – common sense versus scientific thinking	1
1.5	Logical reasoning and decomposition of complex problems	1
1.6	Creativity in research – intelligence versus creativity – creative thinking process and requirements for innovation	1

Module 2 (5 Hours)		
2.1	Importance of literature survey – sources of scientific information: journals, conference papers, patents and technical reports	1
2.2	Techniques for information search using digital databases	1
2.3	Reading, documentation and referencing practices	1
2.4	Integration of research literature and identification of research gaps	1
2.5	Research problem formulation – attributes and sources of research problems – research questions – introduction to problem representation and TRIZ	1
Module 3 (8 Hours)		
3.1	Scientific method and hypothesis formulation	1
3.2	Experimental variables – dependent and independent variables – control and reproducibility in experiments	1
3.3	Precision, accuracy and measurement errors – random and systematic errors	1
3.4	Detection and reduction of experimental errors – statistical treatment and interpretation of experimental data	1
3.5	Principles of design of experiments – experimental documentation	1
3.6	Modelling in engineering research – types of models and stages in modelling	1
3.7	Curve fitting, approximations and mathematical representation of models	1
3.8	Continuum, meso and micro scale modelling approaches – introduction to numerical simulation methods with examples	1
Module 4 (6 Hours)		
4.1	Importance of communication in research – communication process and barriers	1
4.2	Oral communication skills – preparation and delivery of technical presentations – presentation slide design	1
4.3	Scientific writing – structure of technical papers, theses and reports – referencing and citation styles	1
4.4	Scholarly publications – journal selection – peer review process – research metrics	1
4.5	Research ethics – plagiarism, research integrity and ethical publication practices	1
4.6	Intellectual Property Rights – types of IPR – patentability criteria – patent application procedures – technology transfer	1
	Total	**25 hours**

MODEL QUESTION PAPER

QP CODE: Pages: 2

Reg. No.: .....

Name : .....

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS)
KOTHAMANGALAM

FIRST SEMESTER M TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26GE1R105**

Course Name: **RESEARCH METHODOLOGY & IPR**

Max. Marks: 40 Duration: 2 hours

*Answer any **four** questions. Each question carries 10 marks.*

1 a. Explain the stages in the research process and the characteristics of good research. (5 marks)

b. Discuss the role of creative and logical thinking in research with suitable examples from engineering research. (5 marks)

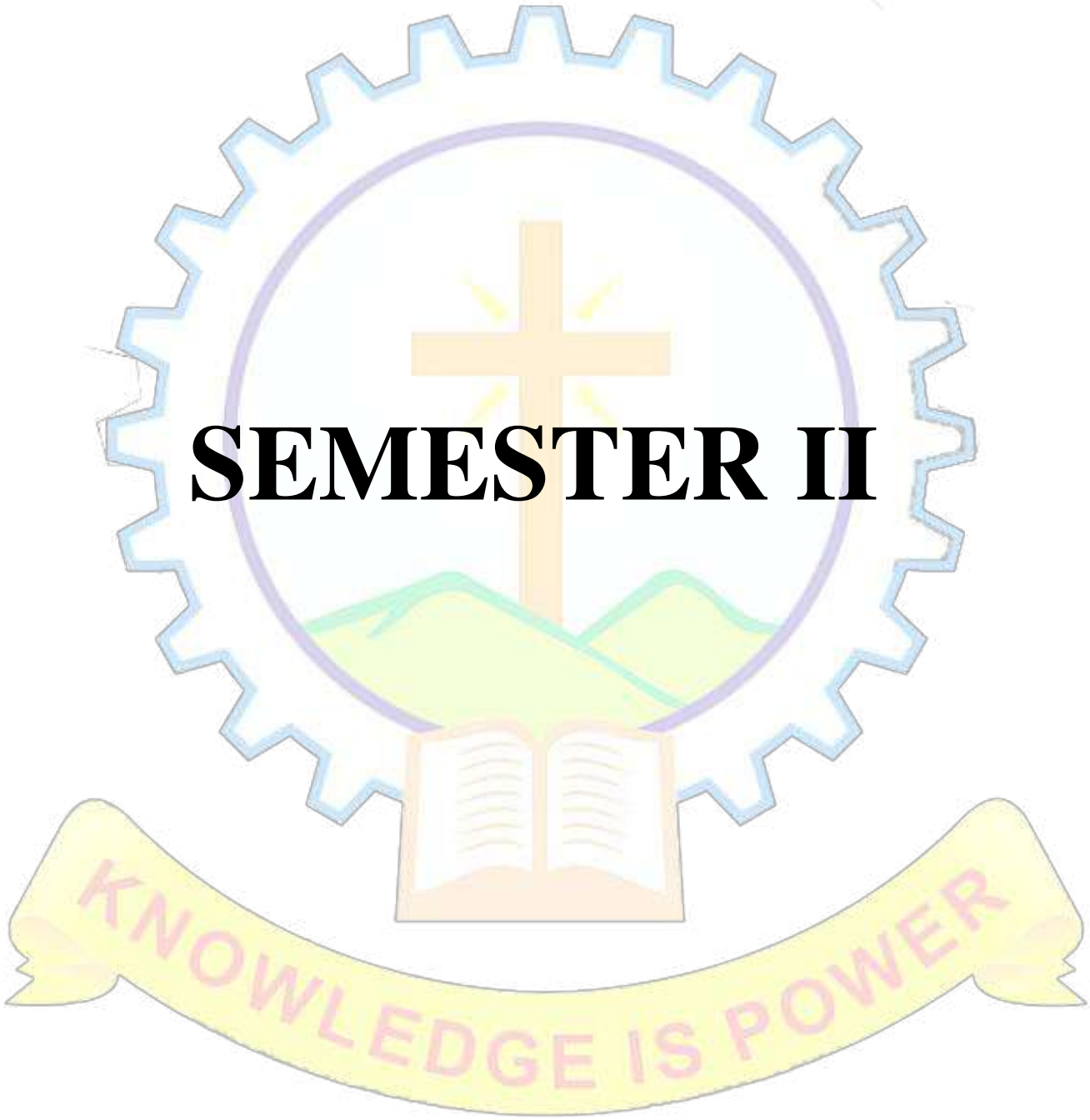
2 a. Describe the methods used for conducting an effective literature survey and the different sources of research information. (5 marks)

b. A researcher intends to study energy efficiency improvement in electric vehicles. Explain how the researcher can identify research gaps and formulate a research problem based on literature survey. (5 marks)

3 a. Explain the scientific method and hypothesis formulation in experimental research. (5 marks)

b. An experiment measures the temperature of a furnace multiple times giving the following readings (°C): 650, 652, 648, 651, 649.
Calculate the mean temperature and comment on the precision of the measurements. (5 marks)

4	a.	Explain the concept and stages of modelling in engineering research.	(6 marks)
	b.	Discuss the importance of approximations and curve fitting in engineering models with examples	(4 marks)
5	a.	Explain the structure of a scientific research paper and the important rules of scientific writing.	(5 marks)
	b.	Discuss the principles for preparing effective technical presentation slides for conferences or seminars.	(5 marks)
6	a.	Explain the peer review process and discuss the criteria used for selecting a suitable journal for publication.	(5 marks)
	b.	Explain the concept of patents, the criteria for patentability, and the steps involved in the patent filing process.	(5 marks)



SEMESTER II

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1D201	Design with Advanced Microcontroller	Discipline Core	3	0	3	6	5

Preamble: In the rapidly evolving landscape of electronics, the demand for high-performance and power-efficient embedded solutions has driven a transition from traditional 8-bit microcontrollers to advanced 32-bit ARM Cortex-M architectures. This course is designed to bridge the gap between fundamental microcontroller interfacing and professional-grade System-on-Chip (SoC) design.

Prerequisite: Digital Electronics, Microprocessor Fundamentals, C Programming, Basic Circuit Theory

Course Outcomes: After the completion of the course, the student will be able to

CO 1	Understand the internal architecture, programmer's model, and memory mapping of the ARM Cortex-M series to optimize embedded software execution. (Level understand)
CO 2	Design and implement robust driver routines for complex peripherals including NVIC, Timers, PWM, and Analog-to-Digital converters. (Level design)
CO 3	Evaluate and Integrate high-speed serial communication protocols (I2C, SPI, CAN) and DMA controllers for efficient data exchange in networked systems. (Level evaluate)
CO 4	Create multi-tasking applications using a Real-Time Operating System while applying low-power management techniques. (Level create)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	1	3	2	3	1
CO 2	2	1	3	3	3	1
CO 3	3	1	3	3	3	2
CO 4	3	2	3	3	3	3

Assessment Pattern

Bloom's Category	Design with Advanced Microcontroller		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember	5	5	5
Understand	20	20	20
Apply	30	30	30
Analyse	30	30	30
Evaluate	10	10	10
Create	5	5	5

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Theory Evaluation : 30 marks

Self-study (Course based task/Seminar/ Quiz/ Micro project) :10 marks

Test paper 1 :10 marks

Test paper 2 :10 marks

Lab Evaluation : 30 marks

Lab work : 10 marks

Final evaluation Test : 20 marks

(Note: 50% of Module 1, 2 and 3 may be considered for each test)

End Semester Examination Pattern:

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions from first three modules, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

Module 1: ARM Cortex-M Architecture & Foundation (10 Hrs)

- **Design Philosophy:** RISC architecture, ARM design evolution, and the Cortex-M product portfolio (M0/M3/M4/M7).
- **Core Internals:** Register bank (R0-R15), special registers (xPSR, PRIMASK), and the operating modes (Thread vs. Handler mode).

- **System Architecture:** Bus Matrix (AHB/APB), memory map overview, the Vector Table, and the Startup Sequence (Reset Handler).
- **GPIO & Basic Interfacing:** Port architecture, configuration registers (MODER, OTYPER, PUPDR), and driving de-initialization.
- **Actuators & Displays:** Practical interfacing techniques for LEDs, Switches, Buzzers, 7-Segment displays, Character LCDs, and Motor control (H-Bridge/Servo/Stepper/Relay).

Module 2: Peripherals & System Management (10 Hrs)

- **Interrupt & Event Handling:** Nested Vectored Interrupt Controller (NVIC), exception priorities, pre-emption, and tail-chaining mechanisms.
- **Timer Units:** SysTick (OS heartbeat), General Purpose Timers (Input Capture/Output Compare), and PWM generation for variable duty cycles.
- **Analog Integration: * ADC:** Successive Approximation, resolution, sampling time, and multi-channel scanning.
    - **DAC:** Basics of digital-to-analog conversion and waveform synthesis.
    - **Sensors:** Interfacing analog sensor types (Ultrasonic, LM35/Humidity/Soil Moisture/PIR).
- **UART Essentials:** Polling-based vs. Interrupt-driven communication and baud rate configuration.

Module 3: Advanced Communication & System Optimization (10 Hrs)

- **High-Speed Communication: * I2C:** Bus protocol, clock stretching, and addressing.
    - **SPI:** Master/Slave modes, full-duplex transmission, and clock polarity/phase (CPOL/CPHA).
    - **CAN:** Industrial bus physical layer and message filtering.
- **Advanced Data Transfer: Direct Memory Access (DMA)**: Principles of offloading the CPU, memory-to-peripheral transfers, and circular buffering for streaming data.
- **RTOS Foundation:** Introduction to real-time concepts (FreeRTOS), task management, scheduling, and basic inter-task communication (semaphores/mutexes).
- **Power Optimization:** Analysis of Low-Power modes (Sleep, Stop, Standby) and techniques for ultra-low-power embedded design.

Module 4: Laboratory Experiments

Foundation & GPIO (Module 1)

1. **LED & Switch Matrix:** Configure GPIOs to read tactile switches and drive an LED pattern using industry-standard driver de-initialization practices.
2. **LCD Interfacing (4-bit Mode):** Write a driver to display alphanumeric strings on a 16x2 LCD without using external libraries.
3. **Motor Control:** Interface a Stepper Motor and a Servo Motor using GPIO sequencing and specialized driver ICs (like the ULN2003 or L298N).

Interrupts, Timers & Analog (Module 2)

4. **Hardware Interrupts (EXTI):** Implement an emergency "Stop" button using the NVIC controller with specific priority levels.
5. **Precise Delay & PWM:** Use a General Purpose Timer to generate a 1kHz PWM signal to control the brightness of an LED or the speed of a DC Motor.
6. **Sensor Data Acquisition:** Interface an Analog Temperature sensor (LM35) and a PIR sensor. Use the ADC to convert voltages and trigger an alarm.
7. **UART Debugging:** Establish full-duplex communication between the Microcontroller and a PC (using a USB-to-TTL converter) in both Polling and Interrupt modes.

Advanced Features & RTOS (Module 3)

8. **I2C/SPI Communication:** Read time/date from an external RTC (Eg: DS1307) via I2C and display it on an OLED screen via SPI.
9. **DMA-backed ADC:** Configure the DMA to move 100 samples of ADC data directly to internal SRAM without CPU intervention.
10. **Multi-Tasking with FreeRTOS:** Create two concurrent tasks:
    - **Task A:** Blink an LED every 500ms.
    - **Task B:** Read a sensor and send data via UART.
    - *Demonstrate pre-emptive scheduling.*

Reference Books

1. Shibu K V —Introduction to Embedded Systems, Tata McGraw Hill Education Private Limited, 2nd Edition
2. Noviello, Carmine. "Mastering STM32."
3. Norris, Donald. Programming with STM32: Getting Started with the Nucleo Board and C/C++. McGraw Hill Professional, 2018.
4. STM32F10xx User Manual
5. Joseph Yiu, The Definitive Guide to the ARM Cortex-M3, Newnes, Second Edition.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Design Philosophy: RISC architecture, ARM design evolution, and the Cortex-M product portfolio (M0/M3/M4/M7).	2
1.2	Core Internals: Register bank (R0-R15), special registers (xPSR, PRIMASK), and the operating modes (Thread vs. Handler mode).	2
1.3	System Architecture: Bus Matrix (AHB/APB), memory map overview, the Vector Table, and the Startup Sequence (Reset Handler).	2
1.4	GPIO & Basic Interfacing: Port architecture, configuration registers (MODER, OTYPER, PUPDR), and driving de-initialization.	2
1.5	Actuators & Displays: Practical interfacing techniques for LEDs, Switches, Buzzers, 7-Segment displays, Character LCDs, and Motor control (H-Bridge/Servo/Stepper/Relay).	2
	Module 2	
2.1	Interrupt & Event Handling: Nested Vectored Interrupt Controller (NVIC), exception priorities, pre-emption, and tail-chaining mechanisms.	2
2.2	Timer Units: SysTick (OS heartbeat), General Purpose Timers (Input Capture/Output Compare), and PWM generation for variable duty cycles.	2
2.3	Analog Integration: * ADC: Successive Approximation, resolution, sampling time, and multi-channel scanning.	2
2.4	DAC: Basics of digital-to-analog conversion and waveform synthesis.	1
2.5	Sensors: Interfacing analog sensor types (Ultrasonic, LM35/Humidity/Soil Moisture/PIR).	1
2.6	UART Essentials: Polling-based vs. Interrupt-driven communication and baud rate configuration.	2
	Module 3	
3.1	High-Speed Communication: * I2C: Bus protocol, clock stretching, and addressing.	2
3.2	SPI: Master/Slave modes, full-duplex transmission, and clock polarity/phase (CPOL/CPHA).	1
3.3	CAN: Industrial bus physical layer and message filtering.	1
3.4	Advanced Data Transfer: Direct Memory Access (DMA): Principles of offloading the CPU, memory-to-peripheral transfers, and circular buffering for streaming data.	2
3.5	RTOS Foundation: Introduction to real-time concepts (FreeRTOS), task management, scheduling, and basic inter-task communication (semaphores/mutexes).	2
3.6	Power Optimization: Analysis of Low-Power modes (Sleep,	2

	Stop, Standby) and techniques for ultra-low-power embedded design.	
	Module 4	
4.1	LED & Switch Matrix: Configure GPIOs to read tactile switches and drive an LED pattern using industry-standard driver de-initialization practices.	1
4.2	LCD Interfacing (4-bit Mode): Write a driver to display alphanumeric strings on a 16x2 LCD without using external libraries.	1
4.3	Motor Control: Interface a Stepper Motor and a Servo Motor using GPIO sequencing and specialized driver ICs (like the ULN2003 or L298N).	1
4.4	Hardware Interrupts (EXTI): Implement an emergency "Stop" button using the NVIC controller with specific priority levels.	1
4.5	Precise Delay & PWM: Use a General Purpose Timer to generate a 1kHz PWM signal to control the brightness of an LED or the speed of a DC Motor.	1
4.6	Sensor Data Acquisition: Interface an Analog Temperature sensor (LM35) and a PIR sensor. Use the ADC to convert voltages and trigger an alarm.	1
4.7	UART Debugging: Establish full-duplex communication between the Microcontroller and a PC (using a USB-to-TTL converter) in both Polling and Interrupt modes.	1
4.8	I2C/SPI Communication: Read time/date from an external RTC (Eg: DS1307) via I2C and display it on an OLED screen via SPI.	1
4.9	DMA-backed ADC: Configure the DMA to move 100 samples of ADC data directly to internal SRAM without CPU intervention.	1
4.10	Multi-Tasking with FreeRTOS: Create two concurrent tasks: Task A: Blink an LED every 500ms. Task B: Read a sensor and send data via UART. Demonstrate pre-emptive scheduling.	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

SECOND SEMESTER M. TECH DEGREE EXAMINATION, MAY 2027

Course Code: **M26EC1D201**

Course Name: **Design with Advanced Microcontroller**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a) Explain the architecture of ARM Cortex-M processors, including register organization, special registers, and operating modes. *(5 Marks)*

   b) Design the startup sequence of an embedded system, explaining the role of the vector table and reset handler with a neat flow diagram. *(5 Marks)*

2.

3. a) Describe the GPIO architecture of STM32 and explain the role of configuration registers (MODER, OTYPER, PUPDR). *(5 Marks)*

   b) Design an interfacing scheme to connect 4 switches, 4 LEDs, and a buzzer. Explain the initialization steps and methods to handle switch debouncing. *(5 Marks)*

4. a) Explain the working of the Nested Vectored Interrupt Controller (NVIC) and interrupt priority mechanism. *(5 Marks)*

   b) Analyze how pre-emption and tail-chaining improve interrupt handling efficiency in real-time systems. *(5 Marks)*

5. a) Explain the working principle of ADC in STM32, including resolution, sampling time, and multi-channel scanning. *(5 Marks)*

   b) Design a system to read temperature using ADC and control a fan using PWM. Explain configuration steps and control logic. *(5 Marks)*

6. a) Compare I2C and SPI protocols in terms of architecture, speed, and communication mechanism. *(5 Marks)*

   b) Evaluate the suitability of CAN protocol for industrial automation systems with justification. *(5 Marks)*

7. a) Explain the concept of Direct Memory Access (DMA) and how it improves system performance. *(5 Marks)*

   b) Design a real-time embedded system using RTOS with DMA support for sensor data acquisition. Include task scheduling and low-power considerations. *(5 Marks)*

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1D202	Design of Power Supplies and Power Conversion Systems	Programme Core	3	0	3	6	5

Preamble: This course introduces the principles and practical design aspects of linear and switching power supplies used in modern electronic systems. It covers voltage regulation, DC-DC converters, magnetics, protection devices, EMI mitigation, and provides hands-on laboratory experiments for designing and testing power converter circuits.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the operation of linear regulators and precision reference devices (Understand).
CO 2	Design DC-DC converters using switching regulator ICs (Apply).
CO 3	Analyse flyback converters, magnetic components, and EMI protection devices (Analyse).
CO 4	Design and implement practical power supply circuits and PCB layouts (Apply / Create).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	1	3	0	0	0
CO 2	2	0	3	3	2	0
CO 3	2	0	3	2	2	0
CO 4	2	2	3	3	3	1

Assessment Pattern

Bloom's Category	Design of Power Supplies and Power Conversion Systems		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	60	60	60
Analyse	20	20	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Theory Evaluation : 30 marks

Self-study (Course based task/Seminar/ Quiz/ Micro project) :10 marks

Test paper 1 :10 marks

Test paper 2 :10 marks

Lab Evaluation : 30 marks

Lab work : 10 marks

Final evaluation Test : 20 marks

(Note: 50% of Module 1, 2 and 3 may be considered for each test)

End Semester Examination Pattern:

The end semester examination should be conducted by the college. The time duration will be 2 Hrs and will contain 6 questions from first three modules, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Linear Regulators and Reference Devices: Basics of regulated power supplies, Linear regulators vs switching regulators, Low Dropout Regulators (LDO), Internal structure, Dropout voltage, Stability issues, Output capacitor requirements, Precision voltage references, Programmable Zener diode – TL431, Internal structure, Reference voltage operation, Error amplifier concept, TL431 as adjustable regulator, TL431 in feedback circuits, Design Example, Design of a regulated 5 V linear power supply for microcontroller applications.

MODULE 2 (10 hours)

Switching DC-DC Converters: Need for switching regulators, Basic topologies, Buck converter, Boost converter, Buck-boost converter, Switching regulator fundamentals, Duty cycle, Inductor current, Output ripple, MC34063 based converter design, Internal architecture, Inductor calculation, Current limiting, Switching frequency, Efficiency considerations, Design Example, Design of a 12 V to 5 V buck converter using MC34063.

MODULE 3 (10 hours)

Flyback Converters, Magnetics and Protection: Flyback Converters, Isolated vs non-isolated converters, Principle of flyback operation, Energy storage in transformer, Primary and secondary current waveforms, Optocoupler feedback using TL431, Transformer and Magnetics, Magnetic materials used in SMPS, Ferrite materials, Core types: EE cores, Core losses and flux density limits, Air gap in flyback transformers, Passive Components in Power Supplies, Capacitors, ESR, ESL, Ripple current rating, Safety capacitors, Inductors, Ferrite vs powdered iron, Saturation current, Protection Devices: MOV, Gas discharge tube, TVS diodes, EMI and Filtering, Common mode choke, EMI filters, Selection of Power Devices, MOSFET selection, Diode selection, Thermal considerations

MODULE 4

List of experiments

1. Study of linear regulators – implementation of 7805 and LDO regulators with measurement of line and load regulation.
2. Study of TL431 programmable reference as an adjustable voltage regulator and feedback control element.
3. Design and implementation of a 12 V to 5 V buck converter using MC34063 with measurement of output ripple and efficiency.
4. Design and implementation of a 5 V to 12 V boost converter using MC34063 with observation of switching waveforms.
5. Study of magnetic cores including identification of ferrite cores (EE16 etc.) and measurement of inductance and saturation characteristics.
6. Study of flyback converter including flyback transformer characteristics and feedback regulation using optocoupler and TL431.
7. Study of EMI filters including LC filter design and testing of common mode choke for noise suppression.
8. Study and testing of protection devices including MOV, TVS diode, and gas discharge tube.
9. Capacitor characterization including measurement of ESR and ripple behaviour.
10. PCB design for switching power supplies through design of a 2-layer DC-DC converter PCB considering high-current loops, ground planes, EMI reduction, and thermal design.

References

1. Abraham I. Pressman, Keith Billings, and Taylor Morey, Switching Power Supply Design, McGraw-Hill.
2. Marty Brown, Practical Switching Power Supply Design, Academic Press.
3. Sanjaya Maniktala, Switching Power Supplies A–Z, Elsevier.
4. L. Umanand, Power Electronics: Essentials and Applications, Wiley India.
5. Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics, Springer.
6. Christophe Basso, Switch-Mode Power Supplies: SPICE Simulations and Practical Designs, McGraw-Hill.
7. Ned Mohan, Tore M. Undeland, and William P. Robbins, Power Electronics: Converters, Applications, and Design, Wiley.
8. Paul Horowitz and Winfield Hill, The Art of Electronics, Cambridge University Press.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Basics of regulated power supplies and classification of power supplies	1
1.2	Linear regulators vs switching regulators	1
1.3	Low Dropout Regulators (LDO): internal structure and operation	1
1.4	LDO characteristics: dropout voltage, stability, output capacitor requirements	1
1.5	Precision voltage references and their applications	1
1.6	Programmable Zener diode – TL431: internal structure	1
1.7	TL431 operation: reference voltage and error amplifier concept	1
1.8	TL431 as adjustable voltage regulator	1
1.9	TL431 in feedback circuits	1
1.10	Design example: 5 V regulated power supply for microcontroller applications	1
	Module 2	
2.1	Introduction to switching regulators and advantages over linear regulators	1
2.2	Basic converter topologies: buck converter	1
2.3	Boost converter operation	1
2.4	Buck-boost converter	1
2.5	Switching regulator fundamentals: duty cycle and switching principles	1
2.6	Inductor current and output ripple in DC-DC converters	1
2.7	MC34063 architecture and working principle	1

2.8	Design procedure using MC34063	1
2.9	Inductor calculation, current limiting and switching frequency	1
2.10	Design example: 12 V to 5 V buck converter using MC34063	1
	Module 3	
3.1	Introduction to isolated converters and flyback topology	1
3.2	Flyback converter operation and energy transfer	1
3.3	Primary and secondary current waveforms	1
3.4	Optocoupler feedback and TL431 regulation	1
3.5	Magnetic materials used in SMPS	1
3.6	Ferrite cores and EE core structures	1
3.7	Core losses, flux density limits and air gap	1
3.8	Passive components in power supplies: capacitors, ESR, ESL and ripple current	1
3.9	Protection devices: MOV, TVS diode, gas discharge tube	1
3.10	EMI and filtering: common mode choke, EMI filters, selection of power devices	1
	Module 4	
4.1	Study of linear regulators – implementation of 7805 and LDO regulators with measurement of line and load regulation.	3
4.2	Study of TL431 programmable reference as an adjustable voltage regulator and feedback control element.	3
4.3	Design and implementation of a 12 V to 5 V buck converter using MC34063 with measurement of output ripple and efficiency.	3
4.4	Design and implementation of a 5 V to 12 V boost converter using MC34063 with observation of switching waveforms.	3
4.5	Study of magnetic cores including identification of ferrite cores (EE16 etc.) and measurement of inductance and saturation characteristics.	3
4.6	Study of flyback converter including flyback transformer characteristics and feedback regulation using optocoupler and TL431.	3
4.7	Study of EMI filters including LC filter design and testing of common mode choke for noise suppression.	3
4.8	Study and testing of protection devices including MOV, TVS diode, and gas discharge tube.	3
4.9	Capacitor characterization including measurement of ESR and ripple behavior.	3
4.10	PCB design for switching power supplies through design of a 2-layer DC-DC converter PCB considering high-current loops, ground planes, EMI reduction, and thermal design.	3

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

SECOND SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1D202**

Course Name: **Design of Power Supplies and Power Conversion Systems**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a) Explain the operation of a linear voltage regulator and discuss the differences between linear and switching regulators.
   b) Explain the internal structure and operation of the TL431 programmable reference device.

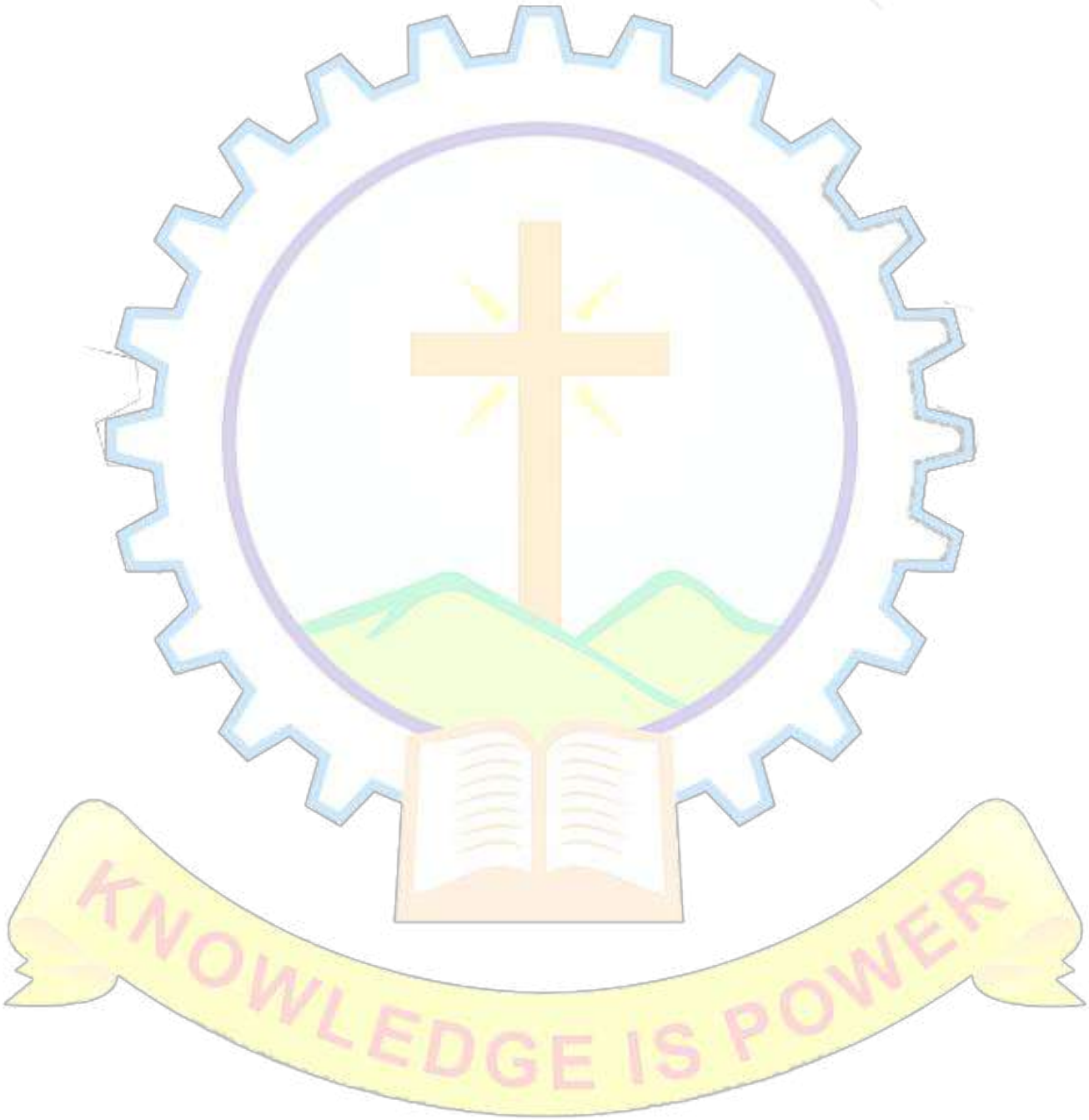
2. a) Design a regulated 5 V power supply using a linear regulator for a microcontroller system. Clearly explain the selection of components.
   b) Using TL431, design an adjustable voltage regulator and derive the expression for output voltage.

3. a) Design a 12 V to 5 V buck converter using MC34063, showing the calculation of inductor value and current limiting resistor.
   b. Design a 5 V to 12 V boost converter using MC34063 and explain the switching waveforms.

4. a) Explain the operation of a flyback converter and illustrate the primary and secondary current waveforms.
   b) Describe the feedback regulation mechanism using optocoupler and TL431 in a flyback power supply.

5. a) Analyse the effect of ESR and ESL of capacitors on the performance of switching power supplies.
   b) Analyse the operation of EMI filters using common mode choke and LC filters in suppressing conducted noise.

6. a) Discuss the role of MOV, TVS diode, and gas discharge tube in surge protection of power supplies.
   b) Analyse the important PCB layout considerations for switching power supplies, including high current loops, grounding, EMI reduction, and thermal design.



CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E203A	Advanced Digital System Design	Elective	4	0	0	5	4

Preamble:

- The student will learn analysis and synthesis of combinational and sequential circuits.
- Learn the principles of digital design and practices using Datapath components such as counters, shift registers and adders.
- To introduce Register Transfer Level (RTL) design.
- The students will learn about optimizations and trade offs in combinational and sequential logic.

Prerequisite:

- Digital system design basics

Course Outcomes: After the completion of the course, the student will be able to

CO 1	Create and analyze combinational and sequential circuits (Bloom's Level: Analyze)
CO 2	Design circuits using data path components such as counters, shift registers and adders (Bloom's Level: Design)
CO 3	Analyze Synchronizer Failure and Metastability (Bloom's Level: Analyze)
CO 4	Understand Register Transfer Level (RTL) design and optimizations in combinational and sequential logic ((Bloom's Level: Understand)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3	2	3	
CO 2			3	3	3	
CO 3	1		3	2	3	
CO 4			3	2	2	1

Assessment Pattern

Bloom's Category	ADVANCED DIGITAL SYSTEM DESIGN		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	40	40	40
Analyze	30	30	30
Evaluate	10	10	10
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course-based task/Micro Project/Data collection and interpretation/Case study : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be drawn from recent technologies in the respective course.

End Semester Examination Pattern:

The end-semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with a minimum of one question from each module, of which the student should answer any four. Each question can carry 10 marks and can have a maximum of 2 subdivisions.

SYLLABUS

MODULE 1 (10 hours)

Combinational Logic Design Principles: Switching Algebra. Combinational-Circuit Analysis, Combinational-Circuit Synthesis. Programmed Minimization Methods, Timing Hazards, Sequential Logic Design Principles: Latches, flip flops, timing and glitches, Finite State Machines, Standard Controller Architecture for Implementing an FSM as a Sequential Circuit.

MODULE 2 (10 hours)

Combinational Circuit Documentation Standards, Datapath Components: Registers, Adders, Comparators, Multiplier—Array-Style, Subtractors and Signed Number, Arithmetic- Logic Units—ALUs, Shifters, Counters and Timers, Register Files.

MODULE 3 (10 hours)

Synchronous Design Methodology- synchronous system structure, Impediments to Synchronous Design: clock skew, gating the clock synchronizer failure, asynchronous inputs, Synchronizer Failure and Metastability, Reliable synchronizer design, Analysis of metastable timing, better synchronizers

MODULE 4 **(10 hours)**

Register-Transfer Level (RTL) Design: High-Level State Machine, C, Determining Clock Frequency, Behavioural-Level Design: C to Gates, Memory Components, Queues, FIFOs, Multiple Processors.

Optimizations and Tradeoffs: Combinational Logic Optimizations and Tradeoffs and Sequential Logic Optimizations and Tradeoffs.

Reference Books

1) Frank Vahid, "Digital Design with RTL Design, VHDL and Verilog", 2/e, Wiley, 2010

2) John F. Wakerly —Digital Design Principles and Practices, 4/e, Prentice Hall, 2005.

3) William James Dally, R. Curtis Harting —Digital Design: A Systems Approach, Cambridge University Press, 2012.

4) Randy H. Katz and Gaetano Borriello —Contemporary Logic Design, 2/E, Prentice Hall India, 2009.

5) Harris & Harris —Digital Design and Computer Architecture, 2/e, Morgan Kaufmann, 2012

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	MODULE 1 (10 Hrs)	
1.1	Combinational Logic Design Principles	
1.1.1	Switching Algebra	0.5
1.2	Combinational-Circuit Analysis	0.5
1.3	Combinational- Circuit Synthesis	1
1.3.1	Programmed Minimization Methods	1
1.4	Timing Hazards	1
1.5	Sequential Logic Design Principles	
1.5.1	Latches, flip flops, timing and glitches	2
1.5.2	Finite State Machines	2
1.5.3	Standard Controller Architecture for Implementing an FSM as a Sequential Circuit	2
	MODULE 2 (10 Hrs)	
2.1	Combinational Circuit Documentation Standards	
2.1.1	Combinational Circuit Documentation Standards	1
2.2	Datapath Components:	
2.2.1	Registers, Adders	2
2.2.2	Comparators, Multiplier – Array style	2
2.2.3	Subtractors and Signed Number, Arithmetic- Logic Units—ALUs	2
2.2.4	Shifters, Counters and Timers, Register Files	3
	MODULE 3 (10 Hrs)	
3.1	Synchronous Design Methodology	
3.1.1	Synchronous system structure	1
3.2	Impediments to Synchronous Design:	
3.2.1	Clock skew	1
3.2.2	Gating the clock synchronizer failure	1
3.2.3	Asynchronous inputs	1
3.3	Synchronizer failure and Metastability	2
3.3.1	Reliable synchronizer design	2
3.3.2	Analysis of metastable timing, better synchronizers	2
	MODULE 4 (10 Hrs)	
4	Register-Transfer Level (RTL) Design	
4.1	High-Level State Machine	2
4.2	RTL Design Process	2
4.3	Determining Clock Frequency	0.5
4.4	Behavioural-Level Design: C to Gates	1
4.5	Memory Components, Queues, FIFOs	2
4.6	Multiple Processors	0.5
4.7	Optimizations and Tradeoffs:	
4.7.1	Combinational Logic Optimizations and Tradeoffs	1
4.7.2	Sequential Logic Optimizations and Tradeoffs	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: M26EC1E203A

Course Name: ADVANCED DIGITAL SYSTEM DESIGN

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Draw a state diagram for an FSM that has an input X and an output Y. Whenever X changes from 0 to 1, Y should become 1 for two clock cycles and then return to 0- even if X is still 1. (Assume that an implicit rising clock is ANDed with every FSM transition condition.) [7 marks]

   b. Trace the behaviour of an SR latch for the following situation: Q, S, and R have been 0 for a long time, then S changes to 1 and stays 1 for a long time, then S changes back to 0. Using a timing diagram, show the values that appear on wires S, R, t, and Q. Assume logic gates have a tiny nonzero delay. [3 marks]

2. a. Create absolute value component abs with an 8-bit input A that is a signed binary number, and an 8-bit output Q that is unsigned and that is the absolute value of A. So if the input is 00001111 (+15) then the output is also 00001111 (+15), but if the input is 11111111 (-1) then the output is 00000001 (+1). [6 marks]

   b. Design a circuit for a 4-bit decrementer. (Component design problem). [4 marks]

3. a. If there is a difference between the arrival times of the clock at different devices, that is an impediment to synchronous design. Discuss with suitable examples and figures. [6 marks]

   b. Discuss acceptable clock gating with example and timing diagrams. [4 marks]

4. Using the five-step RTL design process, design and draw the final implementation of a soda machine dispenser controller. The soda dispenser has three inputs c, s, and a. The 8 –bit input s represents the cost of each bottle of soda. The 1-bit input c is 1 for one clock cycle when a coin is inserted. The output d becomes 1 when the soda should be dispensed i.e. when the value of coins inserted into the soda dispenser is greater than or equal to s. The soda dispenser does not give change.

5. a. There is a system with data inputs W, X, Y, and Z, that should repeatedly output the sum S = W + X + Y + Z. Implement non-pipelined versus pipelined datapaths for the same. [6 marks]

b. Design a 24-bit hierarchical carry-lookahead adder using 4-bit carry-lookahead adders. [4 marks]

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E203B	Sensor Technologies and MEMS	Elective	4	0	0	5	4

Preamble: This course provides a strong foundation in sensor technologies with special emphasis on practical design, interfacing, and integration in VLSI and embedded systems. It covers sensor characteristics, working principles of conventional sensors, signal-conditioning techniques, and advanced MEMS/NEMS devices. The syllabus is deliberately made practical-oriented through case studies, design examples, simulation exercises, and a mandatory micro-project so that students can directly apply the concepts while developing sensor-based embedded or VLSI subsystems.

Prerequisite: Analog Electronic Circuits, Digital System Design, Basic Microelectronics / VLSI Design

Course Outcomes: After the completion of the course the student will be able to

CO1	Analyze static and dynamic characteristics of sensors and select suitable sensors for a given embedded/VLSI application (Analyse)
CO2	Explain the working principles and interfacing requirements of basic resistive, capacitive, inductive, piezoelectric and optical sensors (Understand)
CO3	Design and implement signal-conditioning circuits (amplifiers, filters, bridges, ADC interface) for real-time sensor integration in VLSI/embedded systems (Apply, Create)
CO4	Describe the fabrication processes, design principles and applications of MEMS and NEMS sensors and their integration with CMOS/VLSI (Analyse)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	3	3	2	2	1
CO 2	3	2	3	3	2	1
CO 3	2	3	3	3	3	2
CO 4	3	3	2	2	3	3

Assessment Pattern

Bloom's Category	Continuous Internal Evaluation Tests Test 1 (%Marks)	Test 2 (%Marks)	End Semester Examination (%Marks)
Remember	10	10	10
Understand	20	20	20
Apply	30	30	30
Analyse	30	30	30
Evaluate	5	5	5
Create	5	5	5

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/Data collection and interpretation/Case study : 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern: The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (9 hours)

Sensor Characteristics: Classification of sensors and their role in VLSI and embedded systems. Static characteristics – accuracy, precision, sensitivity, linearity, hysteresis, resolution, repeatability, drift, dead zone. Dynamic characteristics – response time, time constant, frequency response. Error analysis, calibration methods, sensor selection criteria and practical design considerations for embedded/VLSI applications.

MODULE 2 (9 hours)

Basic Sensors: Resistive sensors (strain gauge, potentiometer, RTD, thermistor, LDR), capacitive sensors, inductive sensors (LVDT), piezoelectric sensors, optical sensors (photodiode, phototransistor), temperature sensors (thermocouple, IC sensors), chemical/gas sensors. Working principles, typical specifications, interfacing examples with microcontrollers/FPGA, and case studies in embedded and VLSI-based systems.

MODULE 3 (9 hours)

Signal Conditioning: Need for signal conditioning in sensor-to-VLSI/embedded integration. Instrumentation amplifiers, bridge circuits (Wheatstone, Kelvin), op-amp based amplifiers and filters, linearization techniques, isolation circuits, noise reduction and shielding. ADC interfacing (successive approximation, sigma-delta), sample-and-hold, anti-aliasing filters. Practical design and simulation exercises using tools like LTSpice/Cadence for VLSI/embedded integration.

MODULE 4 (9 hours)

MEMS and NEMS: Scaling laws in MEMS, materials for MEMS/NEMS, fabrication processes (photolithography, bulk/surface micromachining, LIGA, DRIE, thin-film deposition). MEMS sensors – accelerometer, gyroscope, pressure sensor, microphone, flow sensor – design, operation, packaging and CMOS integration. Introduction to NEMS (carbon-nanotube and nanowire based sensors), recent applications in IoT, biomedical and automotive embedded systems.

Reference Books

1. Jacob Fraden, “Handbook of Modern Sensors: Physics, Designs, and Applications”, Fifth Edition, Springer.
2. Tai-Ran Hsu, “MEMS & Microsystems: Design and Manufacture”, Tata McGraw-Hill Education, 2002.
3. Chang Liu, “Foundations of MEMS”, Pearson Education, 2nd Edition.
4. Stephen D. Senturia, “Microsystem Design”, Springer, 2005.

COURSE CONTENTS AND LECTURE SCHEDULE (36 lecture hours)

No	Topic	No. of Lecture/Tutorial hours
	Module 1	
1.1	Introduction, classification and role of sensors in VLSI/embedded systems	2 hrs
1.2	Static characteristics (sensitivity, linearity, hysteresis, resolution, repeatability, etc.)	3 hrs
1.3	Dynamic characteristics, error sources, calibration and sensor selection criteria	4 hrs
	Module 2	
2.1	Resistive, capacitive and inductive sensors – principle & interfacing	3 hrs
2.2	Piezoelectric, optical and thermal sensors with embedded case studies	3 hrs
2.3	Chemical/gas sensors and real-world interfacing examples	3 hrs
	Module 3	
3.1	Amplifiers, filters and bridge circuits for sensor signals	3 hrs
3.2	Instrumentation amplifiers, isolation, noise reduction and ADC interfacing	3 hrs
3.3	Practical design examples and simulation for VLSI/embedded integration	3 hrs
	Module 4	
4.1	MEMS scaling laws, materials and fabrication processes	3 hrs
4.2	Design and operation of key MEMS sensors (accelerometer, gyroscope, pressure sensor)	3 hrs
4.3	NEMS basics, CMOS/VLSI integration and recent applications in IoT/biomedical systems	3 hrs

Model Question Paper

QP CODE: Pages: 2

Reg No.:……..

Name:…….

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

SECOND SEMESTER M. TECH DEGREE EXAMINATION, APRIL 2027

Course Code: M26EC1E203B

Course Name: SENSOR TECHNOLOGIES AND MEMS

Max. Marks: 40 **Duration:** 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. Define the following static characteristics of a sensor: sensitivity, linearity, hysteresis and resolution. Explain their importance in sensor selection for VLSI/embedded applications with suitable examples. (6 marks)

   b. A strain gauge with gauge factor 2.1 and nominal resistance 120 Ω experiences a strain of 500 με. Calculate the change in resistance and discuss the implications on measurement accuracy. (4 marks)

2. a. With neat sketches, explain the construction and working principle of an LVDT. List its advantages and limitations when used in embedded systems. (6 marks)

   b. Compare RTD and thermistor as temperature sensors for a real-time embedded/VLSI application. Which one would you prefer for high-precision applications and why? (4 marks)

3. a. Design a three-op-amp instrumentation amplifier to provide a differential gain of 100 for a bridge sensor outputting a 10 mV signal. Draw the circuit diagram and derive the expression for the overall gain. (7 marks)

   b. Explain the role of an anti-aliasing filter in a sensor signal conditioning chain before ADC interfacing. (3 marks)

4. a. Draw the block diagram of a capacitive MEMS accelerometer and explain its operating principle, including the role of electrostatic actuation/sensing. (5 marks)

   b. List and briefly explain any four key fabrication steps in surface micromachining with suitable diagrams. Highlight its advantages over bulk micromachining. (5 marks)

5. a. Explain the necessity of signal conditioning for a piezoelectric sensor when interfacing with a microcontroller or FPGA. Draw a suitable charge amplifier circuit and derive its output voltage expression. (6 marks)

   b. Differentiate between bulk micromachining and surface micromachining. Give one practical application of each in modern embedded or IoT systems. (4 marks)

6. a. Discuss the scaling laws in MEMS and analyze their impact on sensor sensitivity, power consumption, and integration with CMOS/VLSI technology. (6 marks)

   b. Describe one NEMS-based sensor (e.g., carbon nanotube or nanowire sensor) and evaluate its advantages over conventional MEMS sensors in biomedical or IoT applications. (4 marks)

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E203C	Low Power VLSI	Elective	4	0	0	5	4

Preamble: This course aims to develop students a good knowledge on designing low power VLSI circuits by estimating and analysing power dissipation using different methodologies and there-by implementing low power design methodologies in different levels of design.

Prerequisite: Solid State Devices, VLSI Design, Digital Circuit Design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design chips for battery powered systems and high-performance circuits not exceeding power limits and examine analyze power dissipation. Examine the power dissipation using power analysis like probabilistic Techniques.
CO 2	Design low power circuits at circuit and logic level.
CO 3	Analyze performance management techniques and low power memory design techniques.
CO 4	Understand advanced topics like adiabatic switching.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	2				
CO 2	2	3	1			
CO 3	3	2	2	1		
CO 4	2	3		2	1	

Assessment Pattern

Bloom's Category	Course name		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	20	20	20
Apply	40	40	40
Analyse	30	30	30
Evaluate	10	10	10
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study: 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Need for low power VLSI chips. Introduction - Need for low power VLSI, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, Basic principles of low power design.

Probabilistic Power analysis and Low power Clock Distribution: Probabilistic power analysis: Random logic signals, Probability & frequency, Probabilistic power analysis techniques.

MODULE 2 (10 hours)

Low Power Design- Circuit and Logic level: Circuit level: Transistor & Gate sizing, Network restructuring & reorganization, Special Latches & flip-flops, Logic level: Gate Reorganization, Signal Gating, Logic Encoding.

MODULE 3 (10 hours)

Low power Architecture & Systems: Power & Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Low Power Memory Design: Low power static RAM – organization of static RAM, MOS static RAM cell, Banked organization of SRAMs.

MODULE 4 (10 hours)

Adiabatic switching: Adiabatic switching, Adiabatic charging, Adiabatic amplification, one stage and two stage adiabatic buffer in conventional system, fully adiabatic sequential circuits, stepwise charging, pulsed power supplies.

References

1. Rabaey, Pedram, "Low power design methodologies" Springer Science & Business Media, 2012.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.
4. Anatha P Chandrakasan, Robert W Brodersen, "Low power digital CMOS Design", Kluwer Academic.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
1	**Module 1** **Need for low power VLSI chips and Simulation Power analysis**	**10 hours**
1.1	Introduction - Need for low power VLSI chips	1
1.2	Charging and Discharging capacitance	1
1.3	Short Circuit current in CMOS circuit	1
1.4	CMOS leakage current, Static current	1
1.5	Basic principles of low power design	1
	Probabilistic Power analysis and Low power Clock Distribution	
1.6	Probabilistic power analysis:	1
1.7	Random logic signals	1
1.8	Probability & frequency	1

1.9	Probabilistic power analysis techniques	2
2	**Module 2** **Low Power Design- Circuit and Logic level** **Low power Architecture & Systems**	**10 hours**
2.1	**Low Power Design- Circuit and Logic level**	
2.2	**Circuit level:**	
2.3	Transistor & Gate sizing	1
2.4	Network restructuring & reorganization	2
2.5	Special Latches & flip-flops	2
	Logic level	
2.6	Gate Reorganization	2
2.7	Signal Gating	1
2.8	Logic Encoding	2
	Module 3 **Low Power Architecture and systems**	**10 hours**
	Low power Architecture & Systems	
3.1	Power & Performance Management	1
3.2	Switching Activity Reduction	2
3.3	Parallel Architecture With Voltage Reduction	2
	Low Power Memory Design	
3.4	Low power static RAM – Organization of static RAM	2
3.5	MOS static RAM cell, Banked organization of SRAMs	3
	Module 4 **Adiabatic switching**	**10 hours**
4.1	Adiabatic switching – Adiabatic charging	2
4.2	Adiabatic amplification	2
4.3	One stage and Two stage adiabatic buffer in conventional system	2
4.4	Fully Adiabatic Sequential Circuits	2
4.5	Stepwise Charging	1
4.6	Pulsed Power Supplies	1

Model Question Paper

QP CODE: Pages: 2

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1E203C**

Course Name: **LOW POWER VLSI**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. a. The chip size of a CPU is 15 mm × 25 mm with clock frequency of 300 MHz operating at 3.3 V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 μm and the parasitic capacitance of metal layer is 1 fF/μm^2. What is the power dissipation of the clock signal?

   b. Derive the expression for short circuit power dissipation. Explain the effect of short circuit variation with output load and input slope.

2. a. Define static probability and transition density. Derive the expression for propagation of static probability and transition density in logic circuit.

   b. A system requires high-speed operation with low power. Would you use single edge or double edge-triggered flip-flops? Justify.

3. a. A system designer wants to minimize power consumption without sacrificing throughput. How can parallel architecture with voltage reduction help achieve this?

   b. A logic circuit computes $Y = (A + B) \cdot C$ using a single AND-OR gate with a load of 25 pF, operating at 30 MHz and 1.8 V, with $\alpha = 0.4$. By reorganizing the gate into $Y = A \cdot C + B \cdot C$ using two AND gates and one OR gate, each AND gate drives 10 pF and the OR gate drives 15 pF. Calculate the original and reorganized power dissipation, assuming $\alpha = 0.4$ for all gates.

4. a. Derive an expression for total transition density and explain gate level power analysis.

   b. Discuss about charging and discharging capacitance of CMOS device. Derive an expression for power dissipation.

5. a. Using necessary mathematical equations, explain how you will relate the static probability of a digital signal to switching frequency.

   b. Illustrate how the transistor sizing helps in leakage power reduction.

6. a. Explain how switching activities can be reduced in CMOS digital systems.

   b. Explain adiabatic amplification with a neat diagram. Derive an expression for $E_{load.}$

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1E203D	Embedded Systems for IoT Applications	Elective	4	0	0	5	4

Preamble:

This course introduces the fundamental concepts and system-level aspects of embedded systems for Internet of Things (IoT) applications. It covers embedded hardware and software basics, IoT communication protocols, security mechanisms, and edge intelligence techniques. The course emphasizes understanding the operation of IoT systems and analyzing performance, power, communication, and security trade-offs in real-world embedded IoT deployments.

Prerequisite: NIL

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand embedded system architecture, programming concepts, peripheral interfacing, and real-time operation in IoT nodes. [Understand]
CO 2	Apply IoT communication protocols and networking concepts to evaluate data transmission, protocol selection, and system-level performance in IoT architectures. [Apply]
CO 3	Analyze security requirements of IoT systems and apply appropriate cryptographic and system-level mechanisms to ensure secure communication and device lifecycle management. [Analyze]
CO 4	Apply edge computing and TinyML concepts to evaluate performance trade-offs and analyze hardware–software co-design strategies for efficient IoT systems. [Apply]

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1		2	2	2	
CO 2	1	1	2	3	3	
CO 3	2	1	3	2	3	2
CO 4	2		3	3	3	2

Assessment Pattern

Bloom's Category	Embedded Systems for IoT Applications		
	Continuous Internal Evaluation Tests		End Semester Examination (%Marks)
	Test 1 (%Marks)	Test 2 (%Marks)	
Remember			
Understand	30	30	30
Apply	40	40	40
Analyse	30	30	30
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Self-study (Seminar*) : 10 marks

Course based task/Micro Project/

Data collection and interpretation/Case study: 20 marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

*Seminar should be conducted in addition to the theory hours. Topics for the seminar should be from recent technologies in the respective course.

End Semester Examination Pattern:

The end semester examination will be conducted by the College. Total duration of the examination will be 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks and can have maximum 2 sub-divisions.

SYLLABUS

MODULE 1 (10 hours)

Foundations of Embedded IoT Nodes : Embedded system design flow and toolchains (cross-compilation, linker/startup), microcontroller/SoC basics (memory map, exceptions), embedded C (volatile, bit ops, fixed-width types), peripherals (GPIO, UART, I2C, SPI, ADC/PWM), interrupts, timers, DMA, RTOS basics (tasks, scheduling, synchronization), debugging (watchdog, stack/heap), low-power design, basic performance and energy optimization.

MODULE 2 (10 hours)

IoT Communication and Protocol Stack : IoT architectures (node–gateway–cloud), wireless technologies overview (Wi-Fi, BLE, 802.15.4, LPWAN), TCP/UDP sockets, communication models (pub/sub, request/response), MQTT and CoAP concepts, data encoding (CBOR principles), IPv6/6LoWPAN basics, RPL routing concepts, gateway design, protocol performance (latency, reliability), telemetry design.

MODULE 3 (10 hours)

Secure IoT Systems and Device Lifecycle: Threat modeling, IoT security requirements, lightweight cryptography (hash, MAC, AEAD), device identity and provisioning, TLS/DTLS basics, secure REST (OSCORE concepts), secure boot and root of trust, secure storage, anti-tamper, OTA updates (signing, rollback protection), firmware update architectures, vulnerability management.

MODULE 4 (10 hours)

Edge Intelligence and Hardware Acceleration: Edge vs cloud analytics, TinyML workflow (data, quantization, deployment), embedded inference (TFLite Micro concepts), performance metrics (latency, energy, accuracy), real-time inference constraints, sensor preprocessing, HW–SW co-design, FPGA-based acceleration basics, performance-per-watt analysis, verification and integration.

References

1. Making Embedded Systems: Design Patterns for Great Software — Elecia White, O'Reilly Media, 2nd Edition, 2020.
2. Mastering the FreeRTOS Real Time Kernel — Richard Barry, Real Time Engineers Ltd. (FreeRTOS.org), Latest Edition (~2021).
3. The Definitive Guide to the ARM Cortex-M3 and Cortex-M4 Processors — Joseph Yiu, Newnes (Elsevier), 3rd Edition, 2014 ([IGIET][1])
4. Embedded Systems: Introduction to Arm Cortex-M Microcontrollers — Jonathan W. Valvano, Self-Published, 5th Edition, 2014 ([mgmits.ac.in][2])
5. IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things — David Hanes et al., Cisco Press (Pearson), 1st Edition, 2017 ([SJB INSTITUTE OF TECHNOLOGY][3])
6. Computer Networking: A Top-Down Approach — James F. Kurose, Keith W. Ross, Pearson, 8th Edition, 2021.

7. Practical IoT Security — Brian Russell, Drew Van Duren, Packt Publishing, 1st Edition, 2016.
8. TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers — Pete Warden, Daniel Situnayake, O'Reilly Media, 1st Edition, 2019.
9. FPGA Prototyping by System Verilog Examples — Pong P. Chu, Wiley, 1st Edition, 2017.

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Embedded system design flow, development toolchains (cross-compilation, build systems, linker/startup code), microcontroller/SoC fundamentals (memory map, privilege levels, exception handling)	2
1.2	Embedded C for IoT (volatile keyword, bit manipulation, fixed-width types), register-level programming, memory access techniques	2
1.3	Peripheral interfacing and programming (GPIO, UART, I2C, SPI, ADC, PWM), polling vs interrupt-driven I/O	2
1.4	Interrupts, timers and DMA concepts, event-driven programming	2
1.5	Real-time system concepts (superloop vs RTOS), task scheduling, synchronization (semaphores, mutex), ISR-to-task communication	2
	Module 2	
2.1	IoT system architecture (device–gateway–cloud), layered models and design considerations	2
2.2	Wireless communication technologies (Wi-Fi, BLE, IEEE 802.15.4, LPWAN), trade-offs in power, range and data rate	2
2.3	Transport layer protocols (TCP/UDP), socket programming concepts for embedded systems	2
2.4	Application layer protocols (MQTT – broker, QoS, sessions; CoAP – resources, message types, observe)	2
2.5	Data representation (compact encoding, CBOR principles), IPv6 for constrained devices, 6LoWPAN concepts	1
2.6	Routing (RPL basics), gateway design, telemetry design, protocol performance (latency, reliability, bandwidth)	1
	Module 3	
3.1	IoT threat modeling (assets, trust boundaries, attack models), security requirements and design principles	2
3.2	Lightweight cryptography (hash, MAC, AEAD), need for	2

	constrained-device security	
3.3	Device identity and provisioning (keys, certificates, PSK, manufacturing vs field provisioning)	2
3.4	Secure communication (TLS/DTLS fundamentals, overhead trade-offs, secure session handling)	2
3.5	Secure boot, root of trust, secure storage, anti-tamper mechanisms	1
3.6	OTA firmware updates (signing, rollback protection), firmware lifecycle, vulnerability management	1
	Module 4	
4.1	Edge vs cloud analytics, system-level trade-offs in IoT applications	2
4.2	TinyML workflow (data collection, preprocessing, model selection, quantization, deployment constraints)	2
4.3	Embedded inference (TFLite Micro concepts), real-time inference constraints	2
4.4	Performance evaluation (latency, energy, accuracy), benchmarking methodologies	2
4.5	Hardware–software co-design, sensor preprocessing pipelines, system optimization	1
4.6	FPGA-based acceleration basics, performance-per-watt analysis, verification and system integration	1

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING(AUTONOMOUS), KOTHAMANGALAM

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1E203D**

Course Name: **Embedded Systems for IoT Applications**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. Discuss the importance of embedded C concepts such as volatile, bit manipulation, and fixed-width data types. How do these features help in reliable embedded system design?
2. Describe the concepts of IPv6, 6LoWPAN, and RPL routing. Analyze how they support communication in low-power IoT networks.
3. Explain the concept of IoT threat modeling. Analyze how identifying assets, threats, and attack surfaces helps in improving system security.
4. Describe the TinyML workflow**.** Analyze the challenges involved in deploying machine learning models on embedded IoT devices.
5. Explain the working of MQTT and CoAP protocols. Compare their communication models and analyze which is more suitable for constrained IoT devices.
6. Explain the process of device identity and provisioning in IoT systems. Analyze the differences between using pre-shared keys and certificates.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1S204	Embedded Hardware and Interfacing	Industry Integrated Course	4	0	0	5	4

Preamble: The objective of the course is to equip students with the knowledge and practical skills necessary to design, implement, and troubleshoot FPGA-based systems and control applications so as to make them ready for industry roles in technology and engineering.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Interface FPGAs with LEDs, buzzers, LCDs, optical/PIR sensors, and use ADCs for measuring optical power, temperature, and strain (Blooms Level: Understand, Apply, Analyse)
CO 2	Interface and control relays, solenoids, opto-isolators, motors; implement level control, measurement, and power device interfacing. (Blooms Level: Understand, Apply, Analyse)
CO 3	Implement DFT, FIR, and IIR digital filters. (Blooms Level: Understand, Apply, Analyse)
CO 4	Interface SRAM; design controllers; implement ROM and RAM. (Blooms Level: Understand, Apply, Analyse)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	0	3	2	3	0
CO 2	2	0	3	3	3	1
CO 3	1	0	3	2	3	0
CO 4	1	0	3	2	3	0

Assessment Pattern

Course name	Embedded Hardware and Interfacing		
Bloom's Category	**Continuous Assessment Tests**		**End Semester Examination (%Marks)**
	Test 1 (%Marks)	**Test 2 (%Marks)**	
Remember			
Understand	10	10	10
Apply	40	40	40
Analyse	50	50	50
Evaluate			
Create			

Mark distribution

Total Marks	CIE marks	ESE marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation

Self-study (*Seminar) : 10 marks

Course based task/Seminar/Data collection and interpretation/Case study : 20marks

Test paper 1 (Module 1 and Module 2) : 15 marks

Test paper 2 (Module 3 and Module 4) : 15 marks

End Semester Examination

The examination will be conducted by the College with the question paper provided by the industry. The examination will be for 2 Hrs and will contain 6 questions, with minimum one question from each module of which student should answer any four. Each question can carry 10 marks. The valuation of the answer scripts shall be done by the expert in the industry handling the course.

SYLLABUS

MODULE 1 (10 hours)

Interfacing of FPGA to I/O devices: Interfacing of FPGA to LED, Buzzer, Alphanumeric LCD, Graphical LCD, Optical sensors, and PIR sensors. Principles of Sensor Interfacing and Measurement Techniques, Interfacing of A/D converter and measurement Optical Power, Temperature and Strain.

MODULE 2 (10 hours)

FPGA Based Control: Interfacing Relay, Solenoid Valve and Opto-Isolator, DC Motor Interfacing and Control, Servo and BLDC Motor Interfacing and Control, Stepper Motor Control, Liquid/Fuel Level Control, Voltage and Current Measurement, Power Electronic Device Interfacing and Control.

MODULE 3 (10 hours)

Digital Signal Processing with FPGA: Discrete Fourier Transform, Digital Finite Impulse Response Filter Design, examples, Digital Infinite Impulse Response Filter Design, examples.

MODULE 4 (10 hours)

Interfacing of Memory devices to FPGA: External SRAM: Introduction, Specification of the IS61LV25616AL SRAM, Basic memory controller, a safe design. HDL templates for memory inference, Single port RAM, Dual port RAM, and ROM. Real-world examples.

References

1. A. Arockia Bazil Raj, "FPGA-Based Embedded System Developer's Guide", CRC Press.
2. Pong P. Chu, "FPGA Prototyping by Verilog Examples", John Wiley & Sons, 2008.
3. Shirshendu Roy, "Advanced Digital System Design", Springer
4. Wayne Wolf, 'FPGA-Based System Design' Pearson Education, 2004
5. Zhanyou Sha, Xiaojun Wang, "Optimal Design of Switching Power Supply", Wiley, 2015

COURSE CONTENTS AND LECTURE SCHEDULE

No	Topic	No. of Lecture/ Tutorial hours
	Module 1	
1.1	Introduction to FPGA interfacing and overview of I/O peripherals	1
1.2	Interfacing FPGA with LEDs and buzzers	1
1.3	Interfacing alphanumeric LCD with FPGA	1
1.4	Interfacing graphical LCD and display control techniques	1
1.5	Interfacing optical sensors with FPGA	1
1.6	Interfacing PIR sensors and motion detection systems	1
1.7	Principles of sensor interfacing and measurement techniques	1
1.8	Interfacing A/D converters with FPGA	1
1.9	Measurement of optical power and temperature using ADC	1
1.10	Measurement of strain and other sensor signals with FPGA	1

	Module 2	
2.1	Introduction to FPGA-based control systems	1
2.2	Interfacing relays, solenoid valves and opto-isolators	1
2.3	DC motor interfacing and control techniques	1
2.4	Servo motor interfacing and control using PWM	1
2.5	BLDC motor interfacing and control principles	1
2.6	Stepper motor interfacing and control methods	1
2.7	Liquid and fuel level control systems	1
2.8	Voltage measurement using FPGA-based systems	1
2.9	Current measurement and sensing techniques	1
2.10	Power electronic device interfacing and control using FPGA	1
	Module 3	
3.1	Introduction to Digital Signal Processing using FPGA	1
3.2	Fundamentals of Discrete Fourier Transform (DFT)	1
3.3	Implementation of DFT algorithms using FPGA	1
3.4	Introduction to Digital Filters and applications	1
3.5	Finite Impulse Response (FIR) filter design principles	1
3.6	FIR filter implementation using FPGA	1
3.7	Practical examples of FIR filter design	1
3.8	Infinite Impulse Response (IIR) filter fundamentals	1
3.9	IIR filter implementation using FPGA	1
3.10	Case studies and practical examples of DSP algorithms in FPGA systems	1
	Module 4	
4.1	Introduction to memory interfacing with FPGA	1
4.2	Overview of external SRAM architecture	1
4.3	Specifications of IS61LV25616AL SRAM	1
4.4	Basic SRAM interfacing techniques with FPGA	1
4.5	Design of a basic memory controller	1
4.6	Safe memory controller design considerations	1
4.7	HDL templates for memory inference	1
4.8	Implementation of single-port RAM	1
4.9	Implementation of dual-port RAM	1
4.10	ROM design and real-world memory interfacing examples	1

Model Question Paper

QP CODE: Pages: 1

Reg No.:_____

Name:_____

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM

SECOND SEMESTER M. TECH DEGREE EXAMINATION, DECEMBER 2026

Course Code: **M26EC1S204**

Course Name: **Embedded Hardware and Interfacing**

Max. Marks:40 Duration: 2 hours

Answer any four questions. Each question carries 10 marks.

1. Design a system to interface a graphical LCD (e.g., 128x64 pixels) with an FPGA. Explain the role of a display controller and the memory requirements for storing image data.

2. Design a motion detection system using an FPGA and PIR sensor to trigger an alarm when motion is detected. Provide a detailed block diagram and control logic.

3. Design an FPGA-based system to control the speed and direction of a DC motor using PWM signals. Include a block diagram and describe the control logic.

4. Design an FPGA-based motor drive system using an IGBT-based power electronic interface. Draw the block diagram and explain the working principle.

5. Design an FPGA-based IIR high-pass filter to eliminate low-frequency hum (e.g., 50 Hz) from an audio signal. Include a block diagram and describe the transfer function.

6. Design an FPGA-based memory interface to store sensor data in IS61LV25616AL SRAM for a real-time embedded application. Provide a block diagram and explain the logic.

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M26EC1P205	MINI PROJECT	PROJECT	0	0	4	6	2

Preamble: Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem solving skills.

The introduction of mini projects ensures preparedness of students to undertake dissertation. Students should identify a topic of interest in consultation with PG programme coordinator that should lead to their dissertation/research project. Demonstrate the novelty of the project through the results and outputs. The progress of the mini project is evaluated based on three reviews, two interim reviews and a final review. A report is required at the end of the semester.

Course Outcome

After completing dissertation phase 1 student should be able to

CO1: Identify and define an **Engineering problem**: Students will be able to select a relevant and feasible problem based on real-world needs, demonstrating originality and clarity in problem definition.

CO2: Conduct **Literature review** and develop a **methodology**: Students will develop the ability to critically review and synthesize existing literature to identify research gaps and establish the context for their study.

CO3: Implement the proposed **methodology** and **analyze results**: Students will be able to execute the methodology, develop a prototype/model/simulation, and analyze the results to validate the objectives.

CO4: **Communicate** the project outcomes effectively: Students will be able to prepare a structured report and present the work clearly, demonstrating technical knowledge, understanding, and involvement.

Course Outcome (CO)	Mapped Program Outcome (PO)	Justification
CO1: Identify and define an Engineering problem	PO1: Ability to independently carry out research/investigation and development work	Identifying a research topic requires independent exploration, critical thinking, and decision-making, forming the foundation for research activities.
	PO3: Demonstrate mastery over the specialization area	Topic selection reflects an understanding of advanced concepts beyond undergraduate level.
CO2: Conduct literature review and develop a methodology	PO1: Ability to independently carry out research/investigation and development work	Literature analysis develops the ability to critically evaluate existing work and identify research gaps.
	PO3: Demonstrate mastery over the specialization area	Analyzing literature demonstrates depth of knowledge in the chosen field.
CO3: Implement the proposed methodology and analyze results	PO1: Ability to independently carry out research/investigation and development work	Defining a problem and planning methodology are key steps in executing independent and systematic research.
	PO4: Apply stream knowledge to design or develop solutions for real-world problems	A well-formulated problem and methodology enable the application of domain knowledge to address practical engineering challenges.
	PO5: Identify, select, and apply appropriate techniques, resources, and tools	Developing methodology involves selecting suitable tools, techniques, and resources required for effective problem-solving.
CO4: Communicate the project outcomes effectively	PO2: Ability to communicate effectively, write and present technical reports	Preparing a structured report enhances technical writing, presentation, and communication skills for conveying research ideas clearly.
	PO6: Engage in life-long learning with consideration of sustainability, societal aspects	A proposal often encourages awareness of broader impacts, fostering continuous learning

Continuous Internal Evaluation

The evaluation committee comprises

1. Project coordinator
2. A senior faculty
3. Project supervisor

Course Outcome (CO)	Marks Allocated	Justification
CO1: Identify and define an Engineering problem	25	Topic selection is foundational stage requiring creativity and basic exploration of relevant problems
CO2: Conduct literature review and develop a methodology	25	Literature review is essential for understanding existing work and identifying research gaps through critical analysis.
CO3: Implement the proposed methodology and analyze results	25	Defining the problem is a pivotal step, formulating objectives and methodology demands detailed planning and technical understanding
CO4: Communicate the project outcomes effectively	25	Proposal preparation integrates all prior work into a concise document, focusing on communication
Total	**100**	

Detailed Breakdown and Rationale:

1. **CO1: Identify and define an Engineering problem (25 marks)**
   - This involves identifying a feasible and innovative topic. It's an essential starting point but less complex than subsequent analytical tasks.
   - Assessment: Relevance, originality, and feasibility of the topic.
2. **CO2: Conduct literature review and develop a methodology (25 marks)**
   - A thorough literature review needs significant effort to survey existing work, analyze gaps, and establish context.
   - Assessment: Depth, breadth, and critical evaluation of sources.
3. **CO3: Implement the proposed methodology and analyze results (25 marks)**
   - Involves defining a clear and specific problem, along with formulating objectives and methodology, requiring planning and technical understanding.
   - Assessment: Clarity, specificity, and significance of the problem statement.

4. **CO4: Communicate the project outcomes effectively (25 marks)**
    - The proposal synthesizes all prior work into a structured document. While important for communication, it's less intensive than analysis or planning, hence a slightly lower weight.
    - Assessment: Structure, clarity, and completeness of the proposal

Evaluation Committee - Programme Coordinator, One Senior faculty and Guide.

Sl. No	Type of evaluations	Marks	Evaluation criteria
1	Interim evaluation I	30	Problem identification, literature base, clarity of objectives
2	Interim evaluation II	30	Methodology, progress achieved, depth of knowledge
3	Final evaluation by a committee	25	Completion level and demonstration of functionality/ specifications, clarity of presentation, oral examination, work knowledge and involvement
4	Report	10	The committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level (not more than 25%)
5	Supervisor/Guide	5	Initiative, regularity, involvement
Total Marks		**100**	

Rubrics for Interim Evaluation I (30 Marks)

Parameter	Excellent	Good	Average	Poor
Problem Identification (CO1) (10 marks)	Clearly defined, relevant, innovative, aligned with real-world issues	Relevant but limited innovation	Basic problem, limited relevance	Problem unclear or irrelevant
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Literature Review (CO2) (10 marks)	Comprehensive, recent sources, critical analysis, gap identified	Adequate review with some analysis	Limited sources, mostly descriptive	Very poor or no literature review

Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Clarity of Objectives (CO3) (10 marks)	Well-defined, measurable and achievable	Clear but partially measurable	Vague or broad objectives	Objectives not defined
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)

Rubrics for Interim Evaluation II (30 Marks)

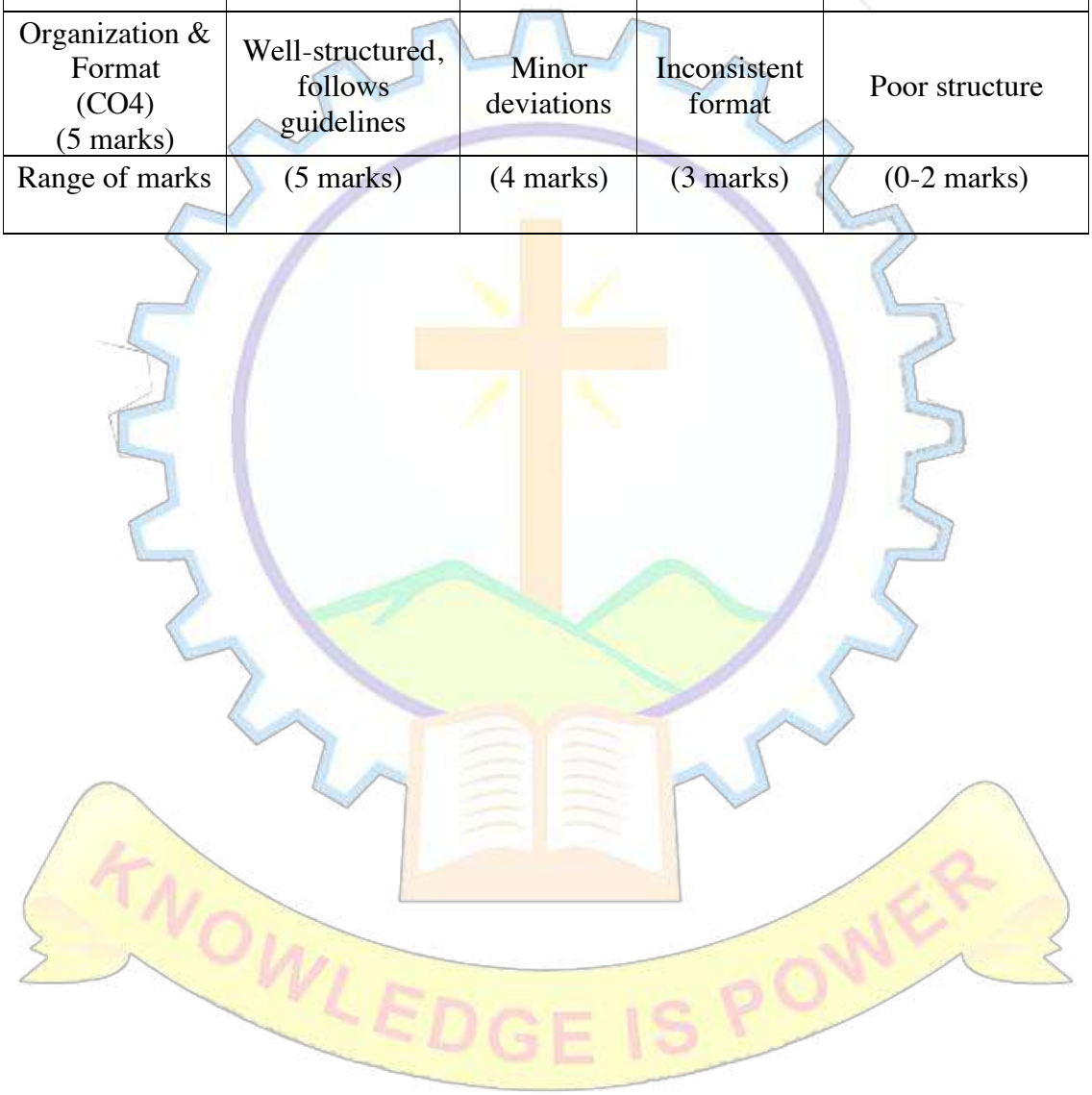
Parameter	Excellent	Good	Average	Poor
Problem statement (CO1) (5 marks)	Clearly defined, relevant, innovative, aligned with real-world issues	Relevant but limited innovation	Basic problem, limited relevance	Problem unclear or irrelevant
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Literature Review (CO2) (5 marks)	Comprehensive, recent sources, critical analysis, gap identified	Adequate review with some analysis	Limited sources, mostly descriptive	Very poor or no literature review
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Methodology (CO3) (5 marks)	Well-structured, appropriate tools/techniques, justified	Suitable methodology with minor gaps	Basic methodology, limited justification	Inappropriate or unclear methodology
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Depth of Knowledge (CO2) (10 marks)	Strong conceptual and technical understanding	Good understanding with minor gaps	Basic understanding	Poor understanding
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Progress Achieved (CO3) (5 marks)	Significant progress with validated results	Moderate progress with partial results	Limited progress	Minimal or no progress
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

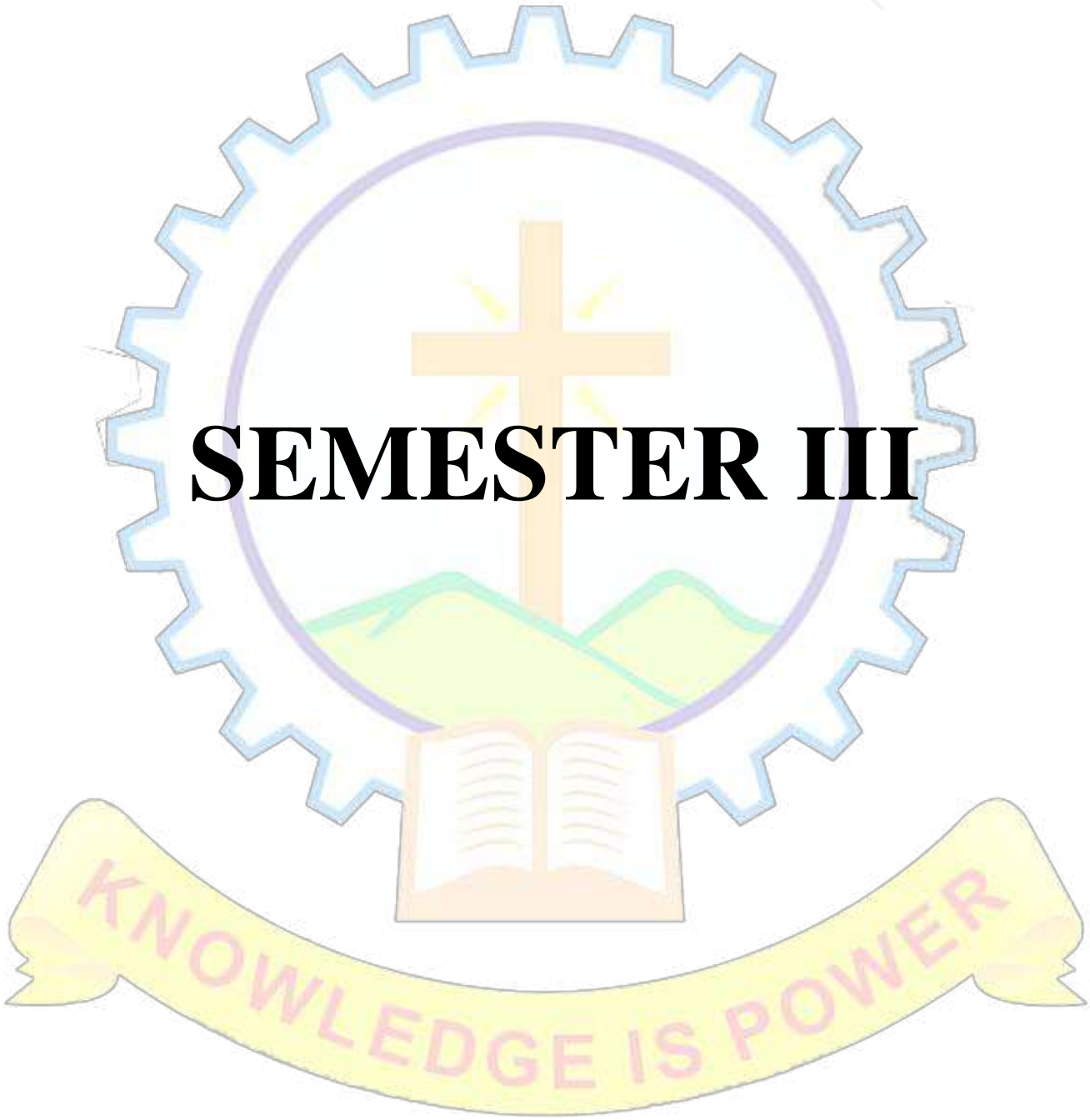
Rubrics for Final Evaluation (25 Marks)

Parameter	Excellent	Good	Average	Poor
Relevance of problem statement (CO1) (5 marks)	Clearly defined, relevant, innovative, aligned with real-world issues	Relevant but limited innovation	Basic problem, limited relevance	Problem unclear or irrelevant
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Implementation of methodology (CO3) (5 marks)	Well-structured, appropriate tools/techniques, justified	Methodology implemented with minor gaps	Basic methodology, limited justification	Inappropriate or unclear methodology
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Knowledge & Involvement (CO4) (10 marks)	Demonstrates good understanding and active involvement throughout the project	Good understanding with consistent involvement	Basic understanding with moderate involvement	Poor understanding; minimal involvement
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Presentation & Viva (CO4) (5 marks)	Clear, confident, logical, excellent responses	Good presentation, answers most questions	Less communication, limited clarity	Poor communication, unable to answer
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Miniproject report (10 Marks)

Parameter	Excellent	Good	Average	Poor
Technical Depth (CO4) (5 marks)	Comprehensive, well-analyzed content	Good technical content	Basic description	Poor/incomplete
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Organization & Format (CO4) (5 marks)	Well-structured, follows guidelines	Minor deviations	Inconsistent format	Poor structure
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)





SEMESTER III

CODE	COURSE NAME	CATEGORY	L	T	P	S	CREDIT
M24EC1M301/ M24EC1M305/ M24EC1M306	**MOOC**	MOOC	0	0	0	0	2

Preamble:

A MOOC course of a minimum 8-week duration must be successfully completed before the end of the fourth semester (starting from Semester 1). The MOOC course shall be considered valid only if it is conducted by AICTE, NPTEL, SWAYAM, or NITTTR. The course must have a minimum duration of 8 weeks and should include syllabus content equivalent to at least 40 hours of teaching. Additionally, it must have a proctored/offline end-semester examination. Students may complete the MOOC course at their convenience but must do so before the end of the fourth semester. The Board of Studies (BoS) will provide a list of approved MOOC courses, provided that at least 70% of the course content aligns with the student's area or stream of study. However, a MOOC course will not be considered if more than 50% of its content overlaps with a core/elective course in the respective discipline or with an open elective. A credit of 2 will be awarded to students who successfully complete the MOOC course as per the evaluation criteria of the respective agency conducting the course.

LIST OF APPROVED MOOC COURSES:

1. Advanced VLSI Design

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: This course explores advanced VLSI design techniques, focusing on submicron design, interconnects, and advanced CMOS technologies for high-performance circuits.
- Relevance: It equips students with cutting-edge knowledge to design next-generation integrated circuits, addressing challenges in modern semiconductor technology.

2. C-Based VLSI Design

- Duration: 8 weeks
- Provider: NPTEL
- Course Content: The course covers high-level synthesis, C-based design methodologies, and scheduling techniques for efficient VLSI system implementation.
- Relevance: It enables students to bridge software and hardware design, enhancing their ability to develop optimized VLSI systems using C-based approaches.

3. Computer Architecture and Organization

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: This course delves into computer architecture concepts, including pipelining, memory hierarchy, and microarchitecture design for efficient processors.
- Relevance: It provides students with essential knowledge for designing and optimizing embedded processors, crucial for system performance.

4. Digital India RISC-V (DIR-V) Processor-based Embedded System Design

- Duration: 65 hours (approximately 8-12 weeks)
- Provider: NIELIT Calicut
- Course Content: The course focuses on designing embedded systems using the RISC-V processor, covering architecture, implementation, and application development.
- Relevance: It is highly relevant for students, offering hands-on experience with RISC-V processors, which are increasingly used in communication and microelectronics applications.

5. Electric Vehicles and Renewable Energy

- Duration: 12 weeks
- Provider: NPTEL (via SWAYAM)
- Course Content: This course examines electric vehicle technology, renewable energy sources for EV charging, battery management systems, and solar/wind integration strategies.
- Relevance: It enables students to design energy-efficient embedded solutions for EV energy management and renewable energy applications.

6. EMI/EMC and Signal Integrity: Principles, Techniques, and Applications

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: The course addresses electromagnetic interference (EMI) mitigation, electromagnetic compatibility (EMC) design, and signal integrity in high-frequency RF circuit design.
- Relevance: It equips students with essential skills to design reliable RF and VLSI systems by addressing electromagnetic interference and ensuring signal integrity in high-frequency

applications.

7. Entrepreneurship Essentials

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: The course provides foundational knowledge on entrepreneurial venture creation and management, addressing key issues faced by entrepreneurs across the enterprise life cycle through a multidisciplinary approach.
- Relevance: It is highly relevant for students, fostering entrepreneurial skills to innovate and manage technology-driven ventures in fields like VLSI and embedded systems.

8. Industrial Electronic Product Design

- Duration: 65 hours (approximately 8-12 weeks)
- Provider: NIELIT Calicut
- Course Content: This course covers the design and development of industrial electronic products, focusing on practical applications and system integration.
- Relevance: It enables students to apply their skills in designing robust electronic products for industrial applications, including communication and microelectronics.

9. Introduction to Machine Learning

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: The course introduces machine learning fundamentals, including supervised and unsupervised learning, algorithms, and their applications in various domains.
- Relevance: It is highly relevant for students, providing skills to integrate machine learning into VLSI signal processing and embedded system applications.

10. Nanobio Technology Enabled Point-of-Care Devices

- Duration: 8 weeks
- Provider: NPTEL
- Course Content: The course focuses on developing portable, ultrasensitive point-of-care systems for healthcare, covering nanobiosensing, signal amplification, electrochemical measurement techniques, and commercialization strategies.

- Relevance: It equips students with skills to design embedded systems and VLSI circuits for portable diagnostic devices, advancing healthcare technology applications.

11. Non-Conventional Energy Resources

- Duration: 12 weeks
- Provider: NPTEL (via SWAYAM)
- Course Content: This course explores renewable energy sources like solar, wind, biomass, geothermal, and ocean energy, along with energy storage and environmental impact analysis.
- Relevance: It provides students with a comprehensive understanding of renewable energy, enabling them to design energy-efficient systems for energy harvesting and management.

12. Real-Time Systems

- Duration: 8 weeks
- Provider: NPTEL
- Course Content: The course covers real-time operating systems (RTOS), scheduling techniques, and embedded applications for time-critical systems.
- Relevance: It is essential for students, equipping them with skills to design and implement real-time systems for applications requiring precise timing and reliability.

13. Solar Energy Engineering and Technology

- Duration: 12 weeks
- Provider: NPTEL (via SWAYAM)
- Course Content: The course examines solar energy technologies, including solar radiation, photovoltaic systems, solar thermal systems, and their design and applications.
- Relevance: It is relevant for students, enabling them to develop embedded solutions for solar power applications and energy-efficient systems.

14. VLSI Design Flow: RTL to GDS

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: This course covers the complete VLSI design flow, including RTL synthesis, Verilog coding, and physical design from RTL to GDSII.
- Relevance: It provides students with end-to-end design skills, essential for creating complex

integrated circuits from concept to fabrication.

15. VLSI Signal Processing

- Duration: 12 weeks
- Provider: NPTEL
- Course Content: The course focuses on digital signal processing (DSP) algorithms, VLSI architectures, and optimization techniques for signal processing applications.
- Relevance: It equips students with the ability to design specialized VLSI architectures for signal processing, enhancing performance in communication and multimedia systems.

16. Advanced Computer Architecture

- Duration: 8 weeks
- Provider: NPTEL
- Course Content: The course focuses on modern computer architecture, covering instruction-level parallelism, pipelining, cache and memory systems, multicore processors, and architectural simulation tools.
- Relevance: It provides essential insights into processor architecture, performance optimization, and memory systems crucial for designing efficient embedded and VLSI systems.

INTERNSHIP

Slot	Course Code	Course	Category	Marks		L-T-P-S	Hours	Credit
K	M26EC1I302	Internship	Internship	50	50	—	-	10

Internship - mandatory internship of minimum 16 weeks duration

Internships are educational and career development opportunities, providing practical experience in a field or discipline. They are structured, short-term, supervised placements often focused around particular tasks or projects with definedtimescales. An internship may be compensated or non-compensated by the organization providing the internship. The internship has to be meaningful and mutually beneficial to the intern and the organization. It is important that the objectives and the activities of the internship program are clearly defined and understood. The internship offers the students an opportunity to gain hands-on industrial or organizational exposure; to integrate the knowledge and skills acquired through the coursework; interact with professionals and other interns; and to improve their presentation, writing, and communication skills. Internship often acts as a gateway for final placement for many students.

A student shall opt for carrying out the Internship at an Industry/Research Organization or at another institute of higher learning and repute (Academia). The organization for Internship shall be selected/decided by the students on their own with prior approval from the faculty advisor/respective PG Programme Coordinator/Guide/Supervisor. Every student shall be assigned an internship Supervisor/Guide at the beginning of the Internship. The training shall be related totheir specialization after the second semester for a minimum duration of 16 weeks. On completion of the course, the student is expected to be able to develop skills in facing and solving the problems experiencing in the related field.

Objectives

- Exposure to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.

- Exposure to the current technological developments relevant to the subjectarea of training.
- Create conducive conditions with quest for knowledge and its applicability on the job.
- Understand the social, environmental, economic and administrative considerations that influence the working environment.
- Expose students to the engineer's responsibilities and ethics.

Benefits of Internship

Benefits to Students

- An opportunity to get hired by the Industry/ organization.
- Practical experience in an organizational setting & Industry environment.
- Excellent opportunity to see how the theoretical aspects learned in classes are integrated into the practical world. On-floor experience provides much more professional experience which is often worth more than classroom teaching.
- Helps them decide if the industry and the profession is the best career optionto pursue.
- Opportunity to learn new skills and supplement knowledge.
- Opportunity to practice communication and teamwork skills.
- Opportunity to learn strategies like time management, multi-tasking etc in an industrial setup.
- Makes a valuable addition to their resume.
- Enhances their candidacy for higher education/placement.
- Creating network and social circle and developing relationships with industry people.
- Provides opportunity to evaluate the organization before committing to afull time position.

Benefits to the Institute

- Build industry academia relations.
- Makes the placement process easier.
- Improve institutional credibility & branding.
- Helps in retention of the students.
- Curriculum revision can be made based on feedback from Industry/students.

- Improvement in teaching learning process.

Benefits to the Industry

- Availability of ready to contribute candidates for employment.
- Year round source of highly motivated pre-professionals.
- Students bring new perspectives to problem solving.
- Visibility of the organization is increased on campus.
- Quality candidate's availability for temporary or seasonal positions andprojects.
- Freedom for industrial staff to pursue more creative projects.
- Availability of flexible, cost-effective workforce not requiring a longterm employer commitment.
- Proven, cost-effective way to recruit and evaluate potential employees.
- Enhancement of employer's image in the community by contributing to the educational enterprise.

Types of Internships

- Industry Internship with/without Stipend
- Govt / PSU Internship (BARC/Railway/ISRO etc)
- Internship with prominent education/research Institutes
- Internship with Incubation centres /Start-ups

Guidelines

- All the students need to go for internship for minimum duration of 16 weeks.
- Students can take mini projects, assignments, case studies by discussing it with concerned authority from industry and can work on it during internship.
- All students should compulsorily follow the rules and regulations as laid by industry.
- Every student should take prior permissions from concerned industrial authority if they want to use any drawings, photographs or any other document from industry.
- Student should follow all ethical practices and SOP of industry.
- Students have to take necessary health and safety precautions as laid by the industry.
- Student should contact his /her Guide/Supervisor from college on weeklybasis to communicate the progress.
- Each student has to maintain a diary/log book

- After completion of internship, students are required to submit
- Report of work done
- Internship certificate copy
- Feedback from employer / internship mentor
- Stipend proof (in case of paid internship).

Total Marks 100: The marks awarded for the Internship will be on the basis of (i)Evaluation done by the Industry (ii)) Internal evaluation & Student's diary (iii) Internship Report and (iv) Comprehensive Viva Voce.

Continuous Internal Evaluation: 50 marks

Internal evaluation & Student's diary	-	25 Marks
Evaluation done by the Industry	-	25 Marks

Internal evaluation committee comprises of Programme coordinator, Project coordinator and a senior faculty.

Student's Diary/ Daily Log: The main purpose of writing daily diary is to cultivate the habit of documenting and to encourage the students to search for details.It develops the students' thought process and reasoning abilities. The students shouldrecord in the daily training diary the day to day account of the observations, impressions, information gathered and suggestions given, if any. It should contain the sketches & drawings related to the observations made by the students. The dailytraining diary should be signed after every day by the supervisor/ in charge of the section where the student has been working. The diary should also be shown to the Faculty Mentor visiting the industry from time to time and got ratified on the day ofhis visit. Student's diary will be evaluated on the basis of the following criteria:

- Regularity in maintenance of the diary
- Adequacy & quality of information recorded
- Drawings, design, sketches and data recorded
- Thought processand recording techniques used
- Organization of the information.

The format of student's diary

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From ..... To .....

Brief description about the nature of internship:

Day	Brief write up about the Activities carried out: Such as design,sketches, result observed, issues identified, data recorded, etc.
1	
2	
3	

Signature of Industry Supervisor *Signature of Section Head/HR Manager*

Attendance Sheet

Name of the Organization/Section:

Name and Address of the Section Head:

Name and Address of the Supervisor:

Name and address of the student:

Internship Duration: From .....To .....

Month & Year		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...
Month & Year																						
Month & Year																						

Signature of Industry Supervisor *Signature of Section Head/HR Manager*

Note:

- Student's Diary shall be submitted by the students along with attendance record and an evaluation sheet duly signed and stamped by the industry to the Institute immediately after the completion of the training.
- Attendance Sheet should remain affixed in daily training diary. Do not remove or tear it off.
- Student shall sign in the attendance column. Do not mark 'P'.
- Holidays should be marked in red ink in the attendance column. Absent should be marked as 'A' in red ink.

Evaluation done by the Industry (Marks 25)

Format for Supervisor Evaluation of Intern

Student Name :_____Date:__ Supervisor Name :_____Designation:__

_____Company/Organization :_____

Internship Address: _____ Dates of Internship: From_____To_____

Please evaluate intern by indicating the frequency with which you observed following parameters:

Parameters	**Marks** Rating (0-10 mark)
Behavior	
Performs in a dependable Manner	
Cooperates with coworkers and supervisor	
Shows interest in work	
Learns quickly	
Shows initiative	
Produces high quality work	
Accepts responsibility	
Accepts criticism	
Demonstrates organizational skills	
Uses technical knowledge and expertise	
Shows good judgment	
Demonstrates creativity/originality	
Analyzes problems effectively	
Is self-reliant	
Communicates well	
Writes effectively	

Has a professional attitude	
Is punctual	
Uses time effectively	

Overall performance of student:

Intern (Tick one): Needs improvement (0 – 1 mark) / Satisfactory (2 mark) / Good (3 mark) / Very Good (4 mark) / Excellent (5 mark)

Additional comments, if any:

Signature of Industry Supervisor *Signature of Section Head/HRManager*

End Semester Evaluation (External Evaluation): 50 Marks

Internship Report - 25 Marks

Viva Voce - 25 Marks

Internship Report: After completion of the internship, the student should prepare a comprehensive report to indicate what he has observed and learnt in the training period and should be submitted to the faculty Supervisor. The student may contact Industrial Supervisor/ Faculty Mentor for assigning special topics andproblems and should prepare the final report on the assigned topics. Daily diary willalso help to a great extent in writing the industrial report since much of theinformation has already been incorporated by the student into the daily diary. The training report should be signed by the Internship Supervisor, Programme Coordinator and Faculty Mentor.

The Internship report (25 Marks) will be evaluated on the basis of following criteria:

- Originality
- Adequacy and purposeful write-up
- Organization, format, drawings, sketches, style, language etc.
- Variety and relevance of learning experience
- Practical applications, relationships with basic theory and concepts taught in the course

Viva Voce (25 Marks) will be done by a committee comprising Project coordinator, Programme Coordinator and an external expert (from Industry or research/academic Institute). This committee will be evaluating the internship report also.

Rubrics for Students diary and Internal Evaluation (25 Marks)

Parameter	Excellent	Good	Average	Poor
Regularity & Completeness (5 marks)	Diary maintained regularly with complete and consistent entries	Mostly regular with minor gaps	Irregular entries; some missing records	Rarely maintained; major gaps
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Application of Concepts (5 marks)	Strong real-world application	Moderate application	Limited application	No application
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Understanding of Work (5 marks)	Thorough understanding, confident	Good understanding	Basic knowledge	Poor understanding
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Organization & Clarity (5 marks)	Well-structured, clear and logical	Minor issues in organization	Poor structure	Disorganized
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Presentation skills (5 marks)	Clear and well structured	Good presentation	Average clarity	Poor communication
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for External Evaluation (Viva Voce) (25 Marks)

Parameter	Excellent	Good	Average	Poor
Understanding of Work (10 marks)	Thorough understanding, confident	Good understanding	Basic knowledge	Poor understanding
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Integration with theory (5 marks)	Strong linkage with academic concepts	Moderate linkage	Weak linkage	No linkage

Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Application of Concepts (5 marks)	Strong real-world application	Moderate application	Limited application	No application
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Presentation skills (5 marks)	Clear and well structured	Good presentation	Average clarity	Poor communicatio n
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Internship report (25 Marks)

Parameter	**Excellent**	**Good**	**Average**	**Poor**
Technical Depth (10 marks)	Comprehensive, well-analyzed, industry relevance	Good technical content	Basic description	Poor/ incomplete
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Organization & Format (10 marks)	Well-structured, follows guidelines	Minor deviations	Inconsistent format	Poor structure
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Originality (5 marks)	Highly original work	Some originality	Limited originality	Copied/ plagiarized
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

DISSERTATION PHASE I

Slot	Course Code	Course	Category	Marks		L-T-P-S	Hours	Credit
				CIE	ESE			
P	M26EC1P303	Dissertation Phase I	Project	100	—	0-0-12-18	12	8

Dissertation Phase I may be undertaken either in the college or in the industry. Dissertation Phase I can be linked with internship. Such students are expected to have the following skills: Technical Skills, Research Skills, Communication Skills, Critical Thinking Skills, and Problem-Solving Skills.

Objectives

The objectives of Phase I of an M.Tech dissertation typically focus on laying a strong foundation for the research work to be conducted in subsequent phases. While specific objectives can vary depending on the institution, discipline, and project, the following are common goals for Phase 1:

1. **Topic Identification and Selection**: To identify a relevant, feasible, and innovative research topic aligned with the student's area of interest and the field's current trends or challenges.
2. **Literature Review**: To conduct a preliminary review of existing research and literature to understand the state of the art, identify gaps, and establish the context for the proposed work.
3. **Problem Definition**: To clearly define the research problem or question that the dissertation aims to address, ensuring it is specific, measurable, and researchable.
4. **Objective Formulation**: To establish clear and achievable objectives for the overall dissertation, outlining what the research intends to accomplish.
5. **Feasibility Assessment**: To evaluate the practicality of the proposed research in terms of available resources, time constraints, and technical requirements.
6. **Methodology Outline**: To develop a preliminary plan for the research methodology, including the tools, techniques, or approaches that will be used to investigate the problem.
7. **Synopsis Preparation**: To prepare and submit a concise synopsis or proposal summarizing the research topic, objectives, significance, and planned approach for approval by the academic supervisor or committee.

8. **Background Knowledge Building**: To deepen the student's understanding of the chosen domain and related concepts, ensuring a solid theoretical foundation for the research.

These objectives are designed to set the stage for Phase 2 and beyond, where the focus typically shifts to implementation, experimentation, and analysis. Phase 1 is critical for ensuring that the research is well-planned and directed toward a meaningful contribution to the field.

Course Outcome

After completing dissertation phase 1 student should be able to

CO1: Demonstrate **Research Topic Selection Skills**: Students will be able to identify and select a research topic that is innovative, relevant, and feasible within the scope of their M.Tech program.

CO2: Conduct **Effective Literature Analysis**: Students will develop the ability to critically review and synthesize existing literature to identify research gaps and establish the context for their study.

CO3: Define **a Clear Research Problem , formulate objectives and methodology**: Students will acquire the skill to articulate a well-defined research problem or question, ensuring it is specific, measurable, and aligned with their dissertation goals.

CO4: Prepare **a Comprehensive Research Proposal**: Students will gain the capability to create a structured synopsis or proposal, effectively communicating the significance, objectives, and planned approach of their research for evaluation.

Course Outcome (CO)	Mapped Program Outcome (PO)	Justification
CO1: Demonstrate Research Topic Selection Skills	PO1: Ability to independently carry out research/investigation and development work	Selecting a research topic requires independent exploration and judgment, aligning with research skills.
	PO3: Demonstrate mastery over the specialization area	Topic selection reflects an understanding of advanced concepts beyond undergraduate level.
CO2: Conduct Effective Literature Analysis	PO1: Ability to independently carry out research/investigation and development work	Literature analysis is a core research skill, requiring independent critical thinking.

Course Outcome (CO)	Mapped Program Outcome (PO)	Justification
	PO3: Demonstrate mastery over the specialization area	Analyzing literature demonstrates depth of knowledge in the chosen field.
CO3: Define a Research Problem, formulate objectives and methodology	PO1: Ability to independently carry out research/investigation and development work	Defining a research problem is a fundamental step in independent research.
	PO4: Apply stream knowledge to design or develop solutions for real-world problems	A well-defined problem often addresses real-world challenges using specialized knowledge.
	PO5: Identify, select, and apply appropriate techniques, resources, and tools	Outlining methodology involves selecting suitable techniques and tools for the research.
CO4: Prepare a Comprehensive Research Proposal	PO2: Ability to communicate effectively, write and present technical reports	Writing a proposal requires clear communication and presentation skills for technical audiences.
	PO6: Engage in life-long learning with consideration of sustainability, societal aspects	A proposal often reflects awareness of broader impacts, fostering

Continuous Internal Evaluation

Evaluation committee comprises of

1. Project coordinator
2. A senior faculty
3. Project supervisor / Industry mentor

Course Outcome (CO)	Marks Allocated	Justification
CO1: Demonstrate Research Topic Selection Skills	25	Topic selection is foundational but less intensive than later stages; it requires creativity and initial research.
CO2: Conduct Effective Literature Analysis	25	Literature review is critical, time-intensive, and requires critical thinking to identify gaps.
CO3: Define a Clear Research Problem; formulate objectives and Methodology	25	Defining the problem is a pivotal step, requiring clarity and alignment with research goals; formulating objectives and methodology demands detailed planning and technical

Course Outcome (CO)	Marks Allocated	Justification
		understanding
CO4: Prepare a Comprehensive Research Proposal	25	Proposal preparation integrates all prior work into a concise document, focusing on communication
Total	**100**	

Detailed Breakdown and Rationale:

1. **CO1: Demonstrate Research Topic Selection Skills (25 marks)**
    - This involves identifying a feasible and innovative topic. It's an essential starting point but less complex than subsequent analytical tasks.
    - Assessment: Relevance, originality, and feasibility of the topic.
2. **CO2: Conduct Effective Literature Analysis (25 marks)**
    - A thorough literature review is a cornerstone of Phase 1, requiring significant effort to survey existing work, analyze gaps, and establish context.
    - Assessment: Depth, breadth, and critical evaluation of sources.
3. **CO3: Define a Clear Research Problem, formulate objectives and methodology (25 marks)**
    - Involves defining a clear and specific research problem and formulating objectives and methodology, requiring critical thinking, planning, and technical understanding as it sets the direction for the dissertation.
    - Assessment: Clarity, specificity, and significance of the problem statement.
4. **CO4: Prepare a Comprehensive Research Proposal (25 marks)**
    - The proposal synthesizes all prior work into a structured document. While important for communication, it's less intensive than analysis or planning, hence a slightly lower weight.
    - Assessment: Structure, clarity, and completeness of the proposal.

M.Tech Dissertation Phase 1 (Industry-Based)

Overview

- **Target Students**: Those who have completed a long-term internship (≥16 weeks) and aim to conduct their dissertation in industry.
- **Focus**: In-depth research, industry-relevant problem-solving, and collaboration with industrial mentors.

- **Total Marks**: 100 (for Phase 1).

Evaluation Process

- **Industry Mentor Involvement**: The industry mentor (from the internship or dissertation site) provides feedback and assesses feasibility.
- **Academic Supervisor**: Ensures academic rigor and alignment with M.Tech standards.
- **Expert Committee Review**: Evaluates the final proposal.
- **Deliverables**:
    - Interim report (literature review, problem statement) – Mid-Phase 1.
    - Final proposal (synopsis) – End of Phase 1.

Evaluation of Dissertation Phase I

Rubrics for Zeroth presentation (30 Marks)

Parameter	Excellent	Good	Average	Poor
Topic Selection (10 marks) (CO1)	Relevant to current research/industry, strong SDG alignment	Relevant with some novelty	Limited relevance	Irrelevant/unclear
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Literature Review & Analysis (10 marks) (CO2)	Comprehensive, recent, critically analyzed; clear research gap	Adequate review with some analysis	Limited, descriptive	Poor/no review
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Problem Definition (5 marks) (CO3)	Clearly defined, specific, research-worthy	Defined but lacks depth	Vague or broad	Not defined
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Presentation & Communication (5 marks) (CO4)	Highly clear, logical, confident delivery	Good clarity	Basic clarity	Poor communication
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Interim presentation (30 Marks)

Parameter	Excellent	Good	Average	Poor
Relevance of Topic (5 marks) (CO1)	Highly innovative, relevant to current research/industry, strong SDG alignment	Relevant with some novelty	Limited relevance	Irrelevant/unclear
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Literature Review & Analysis (10 marks) (CO2)	Comprehensive, recent, critically analyzed; clear research gap	Adequate review with some analysis	Limited, descriptive	Poor/no review
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Objectives & Methodology (10 marks) (CO3)	Well-defined objectives; robust, feasible, justified methodology	Suitable with minor gaps	Basic methodology	Inappropriate/ missing
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Progress Achieved (5 marks) (CO4)	Significant progress with validated results	Moderate progress with partial results	Limited progress	Minimal or no progress
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Final presentation (College based) (40 Marks)

Parameter	Excellent	Good	Average	Poor
Topic Selection & Novelty (10 marks) (CO1)	Topic is highly relevant, innovative, and aligned with current research/ industry needs; clear demonstration of originality	Topic is relevant with some degree of novelty; partial alignment with current trends	Topic is basic with limited originality; minimal relevance to current trends	Topic is outdated, irrelevant, or lacks clarity; no evidence of novelty
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)

Literature Review & Analysis (5 marks) (CO2)	Comprehensive, recent, critically analyzed; clear research gap	Adequate review with some analysis	Limited, descriptive	Poor/no review
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Definition of Research Problem, Formulation of Research (10 marks) (CO3)	Problem is clearly defined, Objectives are clear, measurable, and research-worthy; well-justified with appropriate tools/techniques	Problem is defined and relevant, Objectives are clear; methodology is suitable with minor gaps in justification	Problem is vague, Objectives are basic or partially aligned; methodology is limited or lacks clarity	Problem and objectives are unclear, irrelevant, or not defined
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Report (10 marks) (CO4)	Well-structured, technically sound, excellent clarity, proper references	Good documentation with minor issues	Average documentation	Poor/ incomplete
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Presentation & Communication (5 marks) (CO4)	Highly clear, logical, confident delivery	Good clarity	Basic clarity	Poor communication
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Final presentation (Industry based) (40 Marks)

Parameter	Excellent	Good	Average	Poor
Topic Selection & Novelty (10 marks) (CO1)	Topic is highly relevant, innovative, and aligned with current research/	Topic is relevant with some degree of novelty; partial alignment	Topic is basic with limited originality; minimal relevance to	Topic is outdated, irrelevant, or lacks clarity; no evidence of novelty

	industry needs; clear demonstration of originality	with current trends	current trends	
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Literature Review & Analysis (5 marks) (CO2)	Comprehensive, recent, critically analyzed; clear research gap	Adequate review with some analysis	Limited, descriptive	Poor/no review
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Definition of Research Problem, Formulation of Objectives (5 marks) (CO3)	Problem is clearly defined, Objectives are clear, measurable, and research-worthy; well-justified with appropriate tools/techniques	Problem is defined and relevant, Objectives are clear; methodology is suitable with minor gaps in justification	Problem is vague, Objectives are basic or partially aligned; methodology is limited or lacks clarity	Problem and objectives are unclear, irrelevant, or not defined
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
*Feedback from industry (5 marks) CO3)	Excellent	Good	Satisfactory	Needs improvement
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Report (10 marks) (CO4)	Well-structured, technically sound, excellent clarity, proper references	Good documentation with minor issues	Average documentation	Poor/ incomplete
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Presentation & Communication (5 marks) (CO4)	Highly clear, logical, confident delivery	Good clarity	Basic clarity	Poor communication
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

*Feedback from industry may be taken in 5-point scale

Feedback from Industry (Marks 25)

Format for Supervisor Evaluation of Intern

Student Name :_____Date:__ Supervisor Name :_____Designation:__

_____Company/Organization :_____

Internship Address: _____ Dates of Internship: From_____To_____

Please evaluate intern by indicating the frequency with which you observed following parameters:

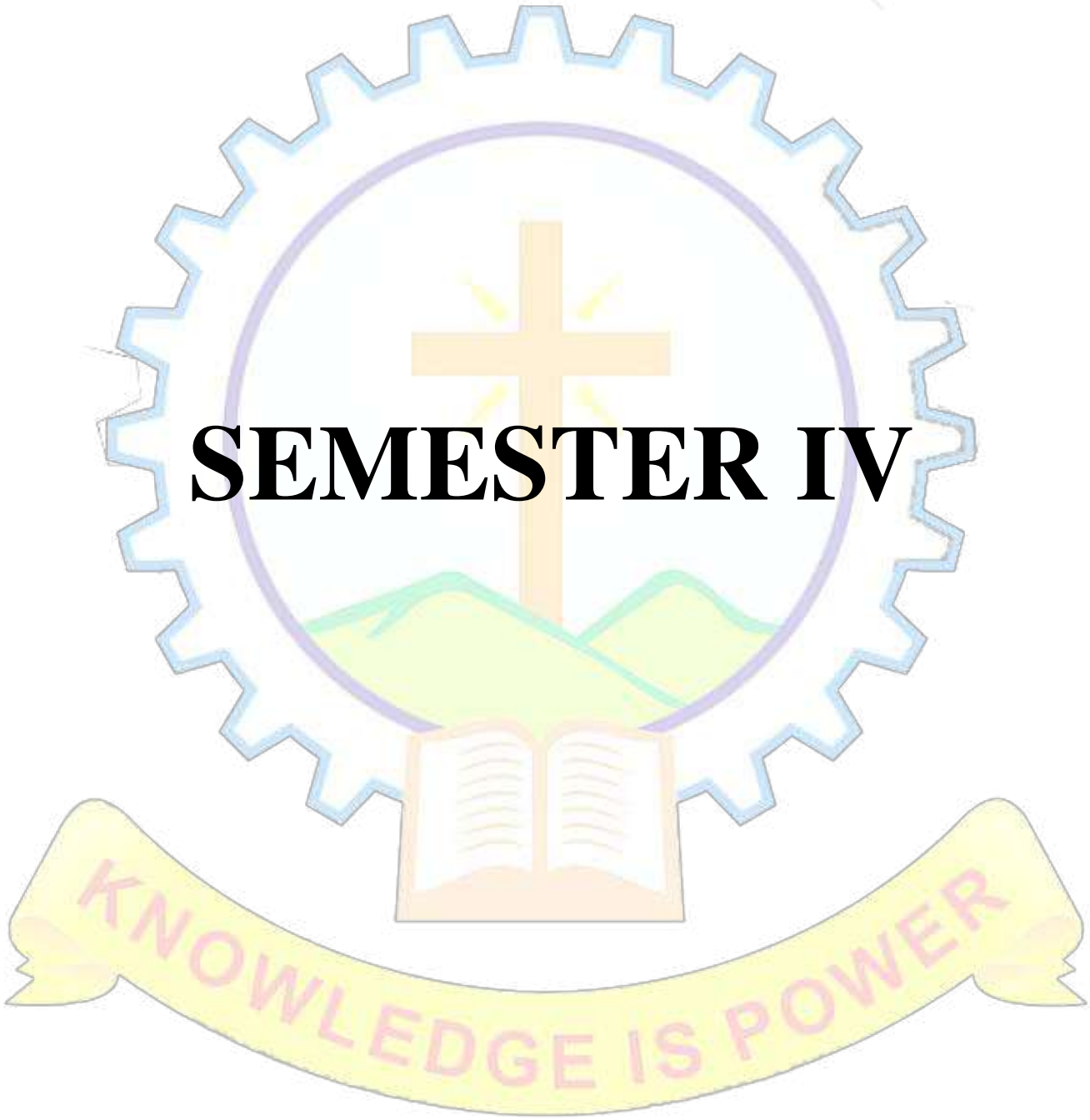
Parameters	**Marks** Rating (0-10 mark)
Behavior	
Performs in a dependable Manner	
Cooperates with coworkers and supervisor	
Shows interest in work	
Learns quickly	
Shows initiative	
Produces high quality work	
Accepts responsibility	
Accepts criticism	
Demonstrates organizational skills	
Uses technical knowledge and expertise	
Shows good judgment	
Demonstrates creativity/originality	
Analyzes problems effectively	
Is self-reliant	
Communicates well	
Writes effectively	
Has a professional attitude	
Is punctual	
Uses time effectively	

Overall performance of student:

Intern (Tick one): Needs improvement (0 – 1 mark) / Satisfactory (2 mark) / Good (3 mark) / Very Good (4 mark) / Excellent (5 mark)

Additional comments, if any:

Signature of Industry Supervisor *Signature of Section Head/HRManager*



SEMESTER IV

DISSERTATION PHASE II

Slot	Course Code	Course	Category	Marks		L-T-P-S	Hours	Credit
				CIE	ESE			
P	M26EC1P401	Dissertation Phase II	Project	100	100	0-0-24-26	24	20
	Total			100	100		24	20

- **Duration**: Typically, the final semester (e.g., fourth semester of M.Tech).
- **Focus**: Implementation, experimentation, analysis, and conclusion of the research initiated in Phase 1.
- **Common Objectives**:
    1. Execute the proposed methodology.
    2. Analyze results and draw meaningful conclusions.
    3. Demonstrate technical proficiency and problem-solving.
    4. Document and present findings effectively.

Scheme for Dissertation Phase II (College-Based)

Course Outcomes (COs)

1. **CO1**: Implement the research methodology proposed in Phase 1 using appropriate tools and techniques (Technical Skills, Problem-Solving Skills).
2. **CO2**: Conduct experiments or simulations to generate data or validate the approach (Research Skills, Critical Thinking Skills).
3. **CO3**: Analyze results and interpret findings to address the research problem (Critical Thinking Skills, Research Skills).
4. **CO4**: Prepare a comprehensive dissertation report that systematically documents the research process, outcomes, and effectively present the work (Communication Skills, Technical Skills).

Evaluation Scheme

1. **Continuous Internal Evaluation (CIE) – 100 Marks**
    - Assessed by the project coordinator throughout the semester.
    - Focus: Progress, effort, and intermediate deliverables.

Paper publication/acceptance (10 marks): Awarded only if at least one paper (authored by the student) is published or accepted in:

- A recognized national/international conference or,
- An indexed journal
- Proof required: Acceptance letter/publication link/DOI/conference proceedings page

Component	Marks	CO Assessed	Justification
Methodology Implementation Progress	25	CO1	Monitors the execution of the proposed plan in a college lab or simulation setup.
Experimental/Simulation Work	25	CO2	Assesses data collection or validation efforts in a controlled academic setting.
Interim Result Analysis	25	CO3	Evaluates preliminary analysis and critical thinking during the semester.
Draft Report Submission, Presentation	25	CO4	Checks documentation quality and adherence to academic standards; assesses communication and ability to discuss progress with the supervisor.
Total	**100**		

Rubrics for Interim Presentation I (30 marks)

Parameter	Excellent	Good	Average	Poor
Implementation of Methodology (10 marks) (CO1)	Methodology implemented	Implementation initiated with good progress	Partial implementation with limited clarity	No meaningful progress
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Experimental/ Analytical Work (10 marks) (CO2)	Results are well-validated and critically analyzed	Results interpreted with some validation	Basic interpretation	No meaningful interpretation
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Validation & Interpretation of Results (5 marks) (CO3)	Strong validation with comparison and justification	Adequate validation	Limited validation	No validation
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Presentation & Viva (5 marks) (CO4)	Excellent communication and defense	Good communication	Average	Poor
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Interim Presentation II (30 marks)

Parameter	Excellent	Good	Average	Poor
Execution of the Proposed Methodology (5 marks) (CO1)	Complete, accurate, well-executed	Minor gaps in execution/accuracy	Partially complete, limited accuracy	Incomplete, incorrect implementation
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Progress Achieved (5 marks) (CO2)	Significant progress with validated results	Moderate progress with partial results	Limited progress	Minimal or no progress
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Quality of Results/Data & Analysis (5 marks) (CO3)	Robust results, deep analysis, strong conclusions	Good results, adequate analysis	Basic results, limited analysis	Weak/invalid results, poor analysis
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Depth of Knowledge (5 marks) (CO3)	Strong conceptual and technical understanding	Good understanding with minor gaps	Basic understanding	Poor understanding
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)
Presentation Skills (5 marks) (CO4)	Highly professional and confident	Good	Average	Poor
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

Rubrics for Final Internal Presentation (40 marks)

Parameter	Excellent	Good	Average	Poor
Proposed Methodology (10 marks) (CO1)	Complete, accurate, well-executed	Minor gaps in execution/ accuracy	Partially complete, limited accuracy	Incomplete, incorrect implementation
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)

Understanding of Work (10 marks) (CO2)	Thorough understanding, confident	Good understanding	Basic knowledge	Poor understanding
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Validation & Results (10 marks) (CO3)	Strong validation with comparison and justification	Adequate validation	Limited validation	No validation
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Report (10 marks) (CO4)	Excellent technical report with proper structure and references	Good clarity	Basic clarity	Poor communication
Range of marks	(9-10 marks)	(7-8 marks)	(5-6 marks)	(0-4 marks)
Presentation skill (5 marks) (CO4)	Clear& confident presentation	Good communication	Average	Poor
Range of marks	(5 marks)	(4 marks)	(3 marks)	(0-2 marks)

2. **End Semester Evaluation (ESE) – 100 Marks**
   - Assessed by a panel (Project coordinator+ supervisor + external examiner) at the semester's end.
   - Focus: Final output, rigor, and presentation.

Component	Marks	CO Assessed	Justification
Final Methodology Implementation	25	CO1	Evaluates the completeness and technical accuracy of the implemented solution.
Quality of Results/Data, Depth of Analysis and Conclusions	30	CO2	Assesses the robustness and validity of experimental or simulation outcomes, examines the interpretation and significance of findings.
Final Dissertation Report	20	CO3	Judges the quality, structure, and clarity of the written report.
Viva Voce/Presentation	25	CO4	Tests the ability to defend work and communicate findings to an

Component	Marks	CO Assessed	Justification
			academic panel.
Total	**100**		

Rubrics for End Semester Evaluation

Parameter	Excellent	Good	Average	Poor
Methodology Implementation (25 marks) (CO1)	Complete, accurate, well-executed	Minor gaps in execution/accuracy	Partially complete, limited accuracy	Incomplete, incorrect implementation
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)
Quality of Results/Data & Analysis (30 marks) (CO2)	Robust results, deep analysis, strong conclusions	Good results, adequate analysis	Basic results, limited analysis	Weak/invalid results, poor analysis
Range of marks	(25-30 marks)	(20-24 marks)	(10-19 marks)	(0-9 marks)
Dissertation Report (20 marks) (CO3)	Clear, well-structured, high quality	Good structure with minor issues	Adequate but lacks clarity/flow	Poorly written, unstructured
Range of marks	(15-20 marks)	(10-14 marks)	(5-9 marks)	(0-4 marks)
Viva Voce / Presentation (25 marks) (CO4)	Confident, clear, presentation with in-depth knowledge	Clear with minor gaps	Basic explanation, weak defense	Unclear, unable to defend
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)

Scheme for Dissertation Phase II (Industry-Based)

Course Outcomes (COs)

1. **CO1**: Implement the industry-oriented methodology proposed in Phase 1 using industry tools/resources (Technical Skills, Problem-Solving Skills).
2. **CO2**: Perform industry-relevant experiments, validations, or prototypes (Research Skills, Critical Thinking Skills).
3. **CO3**: Analyze results and draw conclusions applicable to the industry problem (Critical Thinking Skills, Research Skills).

4. **CO4:** Prepare a comprehensive dissertation report that systematically documents the research process and outcomes, and effectively present and defend the work before an academic audience (Communication Skills, Technical Skills).Evaluation Scheme

1. **Continuous Internal Evaluation (CIE) – 100 Marks**
   - Assessed jointly by the Project coordinator, supervisor/industry mentor during the semester.
   - Focus: Industry collaboration, progress, and practical application.

Component	Marks	CO Assessed	Justification
Methodology Implementation Progress	25	CO1	Tracks execution of the plan in an industry environment using real-world tools.
Industry Validation/Prototype Work, result Analysis	30	CO2	Evaluates practical outputs (e.g., prototypes, tests) relevant to industry needs, and assesses industry-applicable insights derived during the process.
Draft Report Submission	20	CO3	Ensures documentation meets both academic and industry standards.
Industry Feedback/Interaction	25	CO4	Gauges communication with the industry mentor and progress updates.
Total	**100**		

Rubrics for Internal Evaluation (100 marks)

Parameter	Excellent	Good	Average	Poor
Methodology Implementation (25 marks) (CO1)	Systematic, on-time, effective use of tools	Good progress, minor gaps	Partial progress, some delays	Poor progress, inadequate execution
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)
Industry Validation / Prototype & Analysis (30 marks) (CO2)	High-quality validation, deep analysis, strong relevance	Good validation and analysis	Basic validation, limited analysis	No meaningful validation or analysis
Range of marks	(25-30 marks)	(20-24 marks)	(10-19 marks)	(0-9 marks)

Draft Report (20 marks) (CO3)	Clear, structured, comprehensive	Good with minor issues	Adequate, lacks depth/clarity	Poor, incomplete, unstructured
Range of marks	(15-20 marks)	(10-14 marks)	(5-9 marks)	(0-4 marks)
Industry Feedback / Interaction (25 marks) (CO4)	Proactive, regular updates, effective feedback use	Good interaction, periodic updates	Limited interaction, partial feedback use	Poor communication, no feedback use
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)

Feedback from Industry (Marks 25)
Format for Supervisor Evaluation of Intern

Student Name :_____Date:__ Supervisor Name :_____Designation:__

_____Company/Organization :_____

Internship Address: _____ Dates of Internship: From_____To_____

Please evaluate the intern by indicating the frequency with which you observed following parameters:

	Parameters	**Marks** Rating (0-10 mark)
Overall	Behavior	
	Performs in a dependable Manner	
	Cooperates with coworkers and supervisor	
	Shows interest in work	
	Learns quickly	
	Shows initiative	
	Produces high quality work	
	Accepts responsibility	
	Accepts criticism	
	Demonstrates organizational skills	
	Uses technical knowledge and expertise	
	Shows good judgment	
	Demonstrates creativity/originality	
	Analyzes problems effectively	
	Is self-reliant	
	Communicates well	
	Writes effectively	
	Has a professional attitude	
	Is punctual	
	Uses time effectively	

performance of the student:

Intern (Tick one): Needs improvement (0 – 1 mark) / Satisfactory (2 mark) / Good (3 mark) / Very Good (4 mark) / Excellent (5 mark)

Additional comments, if any:

Signature of Industry Supervisor *Signature of Section Head/HR Manager*

2. **End Semester Evaluation (ESE) – 100 Marks**
    - Assessed by a panel (Project coordinator, supervisor/industry mentor, external examiner).
    - Focus: Final deliverables, industry relevance, and dual-audience presentation.
    -

Component	Marks	CO Assessed	Justification
Final Methodology Implementation	25	CO1	Evaluates the technical success of the industry-implemented solution.
Quality of Industry Outputs/Results, depth of Analysis and Industry Impact	30	CO2	Assesses the practical utility and quality of industry-specific deliverables, examines conclusions and their relevance to industry challenges.
Final Dissertation Report	20	CO3	Judges the report's ability to address academic rigor and industry needs.
Viva Voce/Presentation (Dual Audience)	25	CO4	Tests communication to both academic and industry evaluators.
Total	**100**		

Rubrics for End Semester Evaluation (100 marks)

Parameter	Excellent	Good	Average	Poor
Methodology Implementation (25 marks) (CO1)	Innovative, well-executed, validated	Appropriate, minor gaps	Acceptable, limited depth/validation	Poor, unclear, or irrelevant
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)

Results, Analysis & Industry Impact (30 marks) (CO2)	Highly relevant, deep analysis, strong impact	Relevant, good analysis	Limited relevance, basic analysis	Irrelevant, weak/no analysis
Range of marks	(25-30 marks)	(20-24 marks)	(10-19 marks)	(0-9 marks)
Final Dissertation Report (20 marks) (CO3)	Well-structured, clear, technically strong	Good structure, minor issues	Adequate, lacks clarity/depth	Poorly written, unstructured
Range of marks	(15-20 marks)	(10-14 marks)	(5-9 marks)	(0-4 marks)
Viva Voce / Presentation (25 marks) (CO4)	Confident, clear, presentation with in-depth knowledge	Clear with minor gaps	Basic, limited clarity	Unclear, unable to defend
Range of marks	(20-25 marks)	(15-19 marks)	(10-14 marks)	(0-9 marks)

EVALUATION COMMITTEES AT A GLANCE

MINI PROJECT (100 Marks)

Continuous Internal Evaluation (CIE) – 100 Marks

The evaluation committee comprises the project coordinator, senior faculty and the project supervisor. Final evaluation by a Committee of the Project coordinator, Project supervisor and a senior faculty.

INTERNSHIP (100 Marks)

Internal evaluation committee (25 Marks) comprises the Program coordinator, Project coordinator and a senior faculty.

Viva Voce (25 Marks) will be done by a committee comprising the Program Coordinator, Project coordinator and an external expert (from Industry or research/academic Institute)

DISSERTATION PHASE I (100 Marks)

Continuous Internal Evaluation (CIE) – 100 Marks

Evaluation committee comprises of Project coordinator, senior faculty and the project supervisor / Industry mentor

DISSERTATION PHASE II (200 Marks)

Continuous Internal Evaluation (CIE) – 100 Marks

Assessed jointly by the Project coordinator, supervisor / industry mentor and senior faculty during the semester.

End Semester Evaluation (ESE) – 100 Marks

Assessed by a panel of Project coordinator, supervisor and external examiner at the semester end.